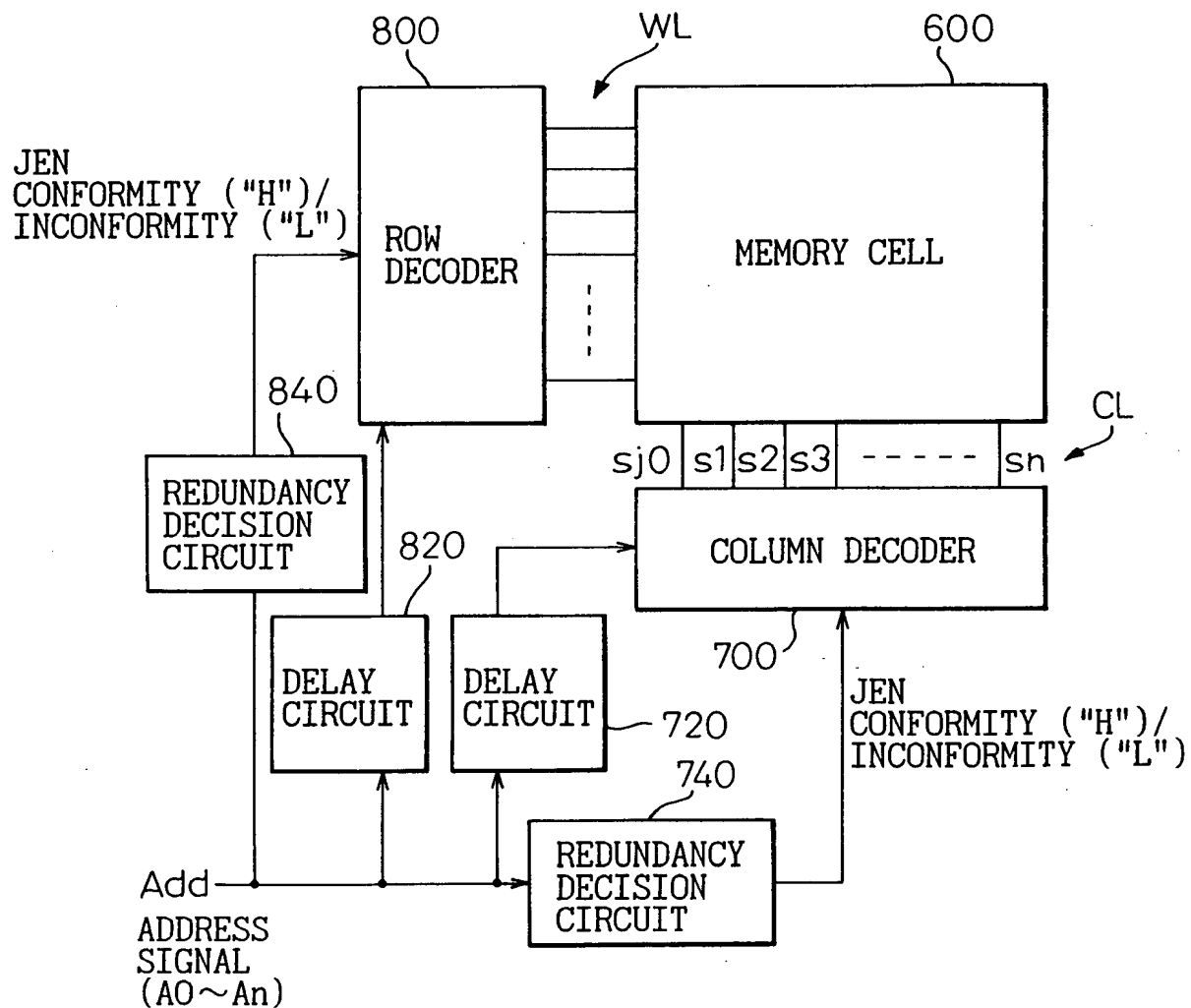




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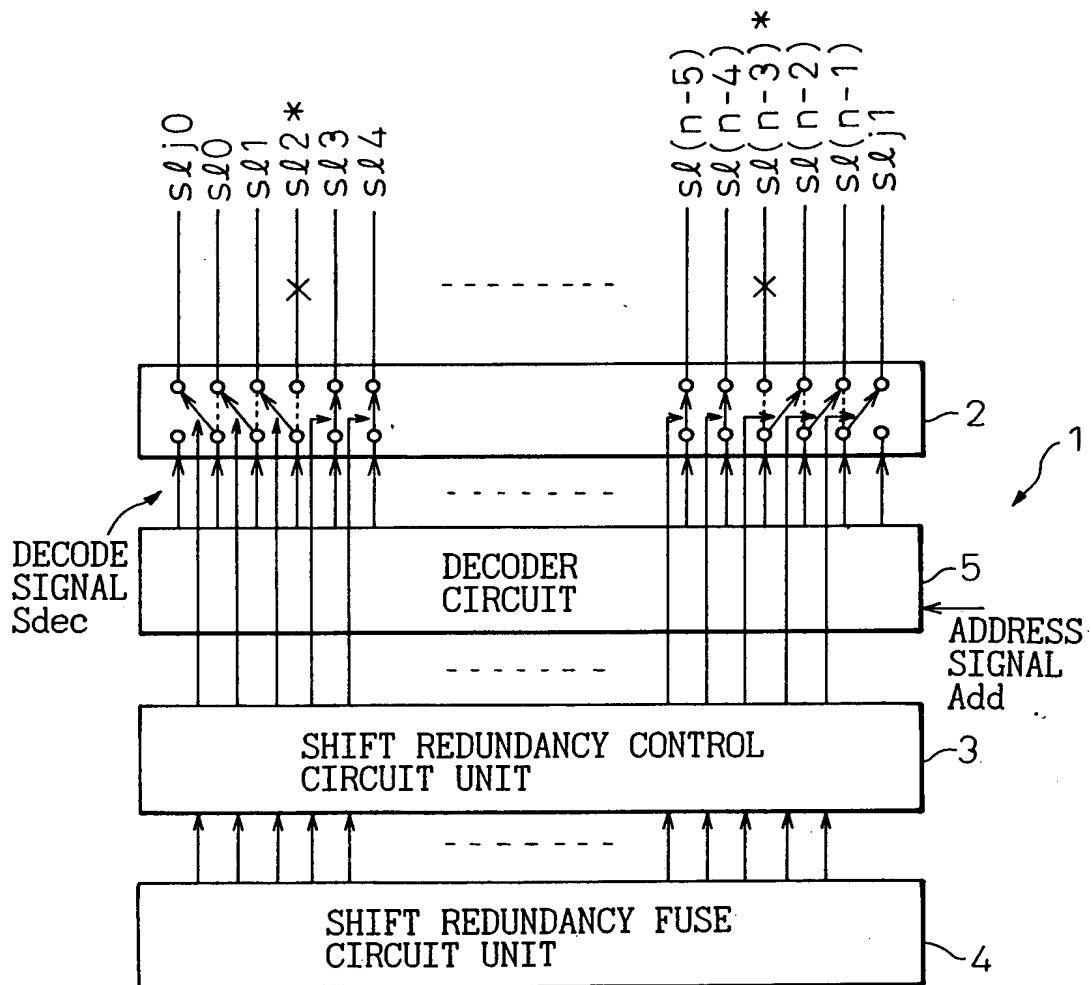
Fig.1





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Fig.2

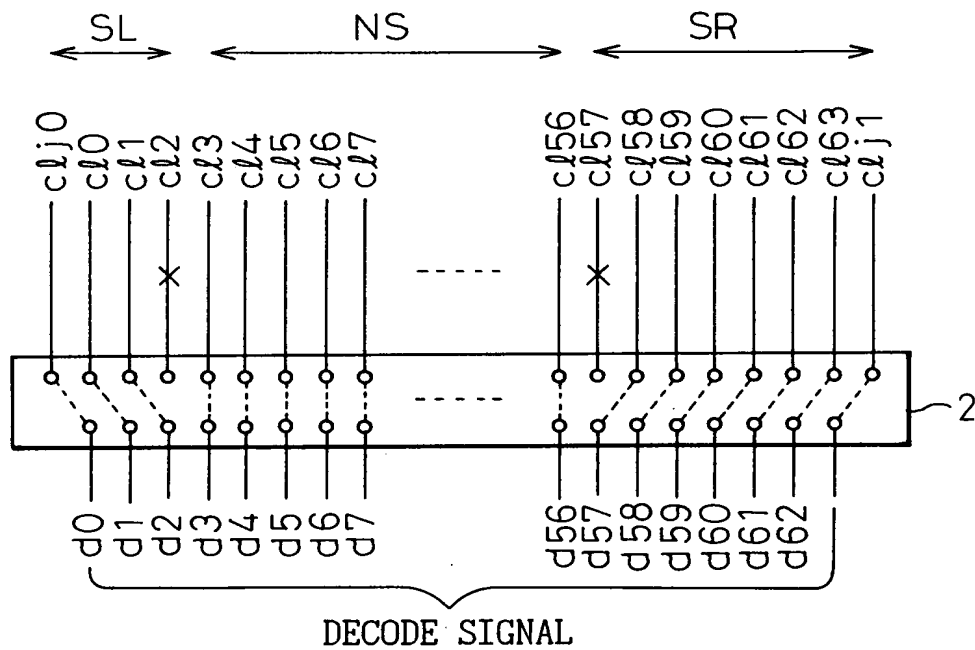


REMARKS)
 FOR EXAMPLE, IT IS ASSUMED THAT
 FAULT HAS OCCURRED IN EACH OF
 SELECTING LINES $sl2$ AND $sl(n-3)$



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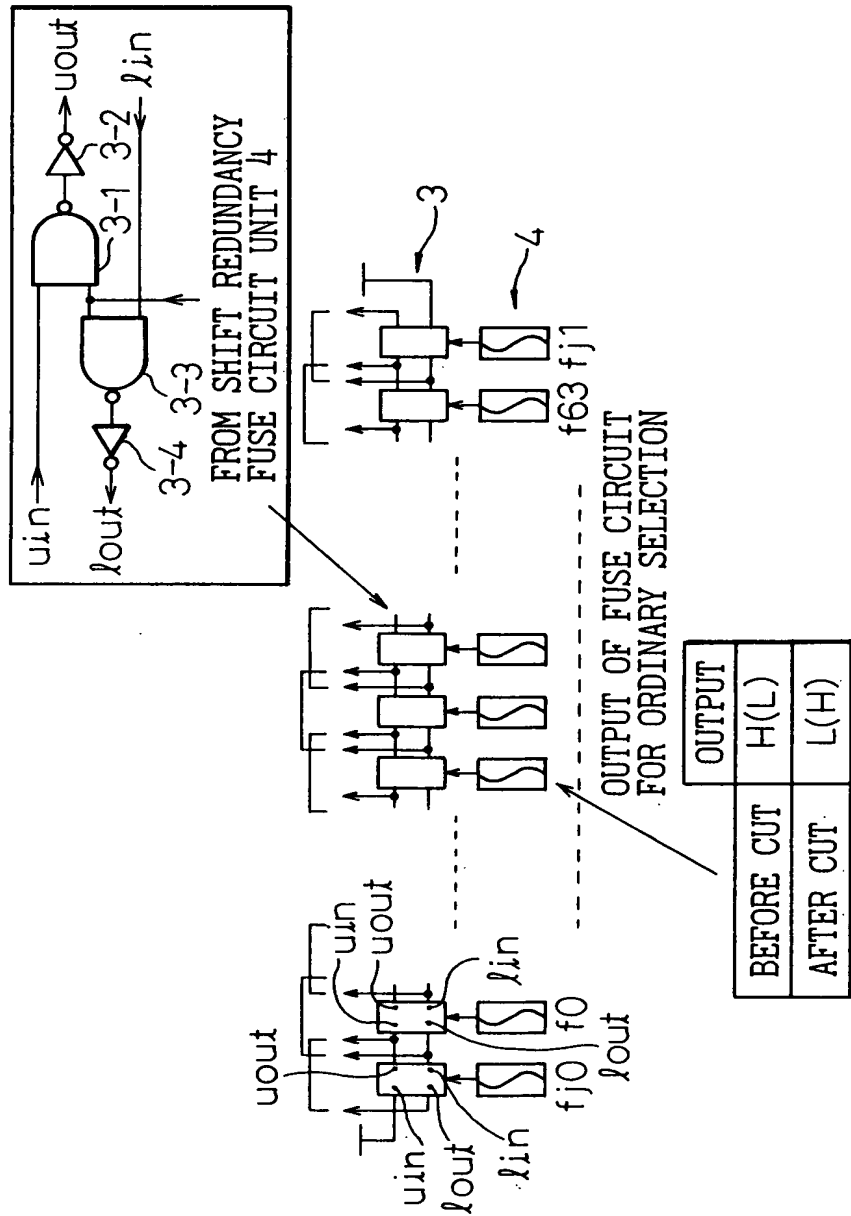
Fig. 3





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Fig. 4



REMARKS)
 "L" OR "H" IN PARENTHESES REPRESENTS OUTPUT OF FUSE
 CIRCUIT FOR REDUNDANCY SELECTION

TWO FUSES BLOW/ONE REDUNDANCY



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Fig.5a

SHIFT	NS															
uout	L	L	L	L	-----	L	L	L	L							
lout	L	L	L	L	-----	L	L	L	L							
OUTPUT OF SHIFT REDUNDANCY FUSE CIRCUIT UNIT	L	H	H	H	-----	H	H	H	L							
	↑	↑	↑	↑		↑	↑	↑	↑							
	fj0	f0	f1	f2		f61	f62	f63	fj1							

Fig.5b

SHIFT	NON-SELECTION															
	SL				NS											
uout	H	H	L	L	-----	L	L	L	L							
lout	L	L	L	L	-----	L	L	L	L							
OUTPUT OF SHIFT REDUNDANCY FUSE CIRCUIT UNIT	H	H	L	H	-----	H	H	H	L							
	↑	↑	↑	↑		↑	↑	↑	↑							
	fj0	f0	f1	f2		f61	f62	f63	fj1							

Fig.5c

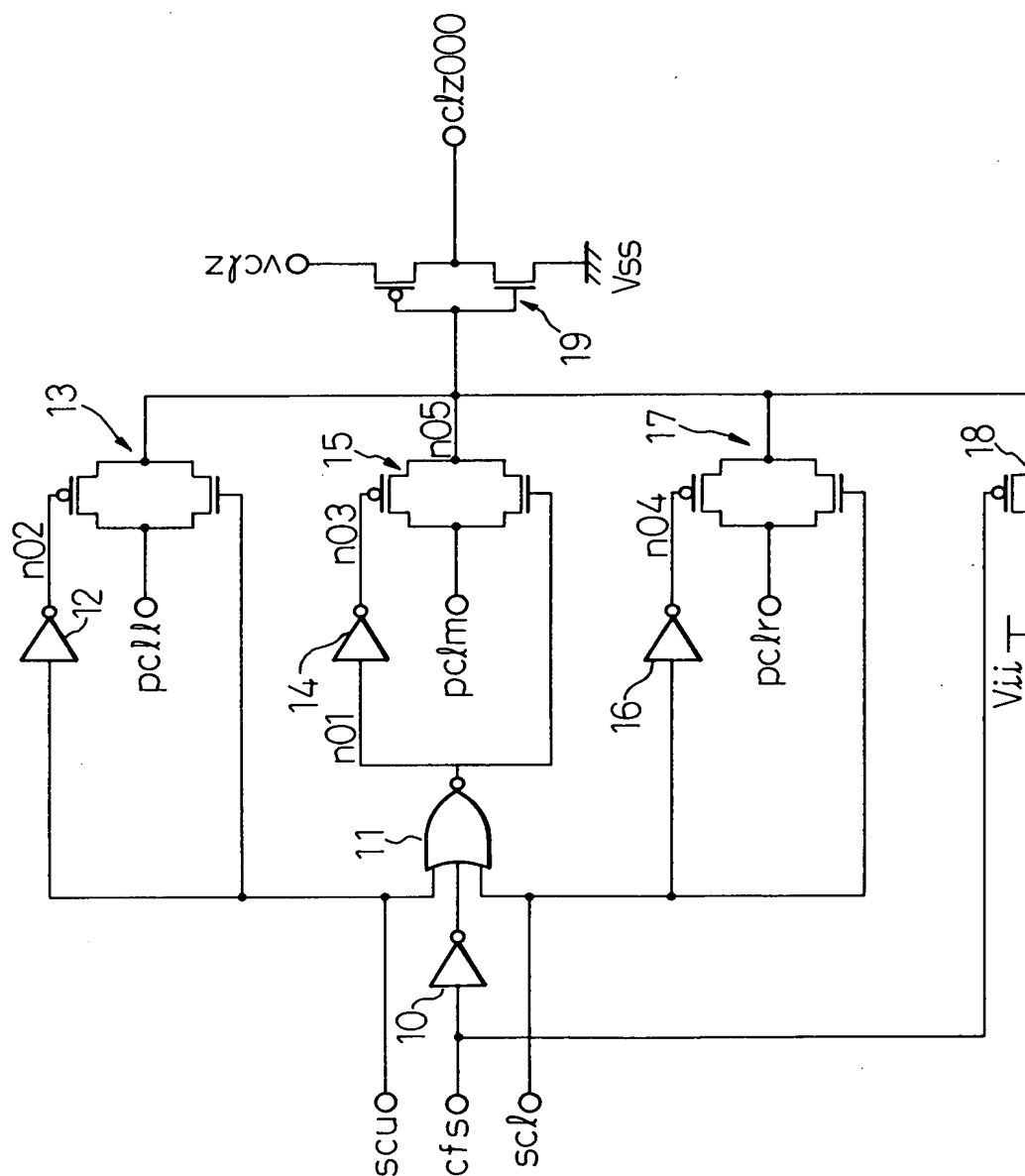
SHIFT	NON-SELECTION								NON-SELECTION							
	SL				NS				SR							
uout	H	H	L	L	-----	L	L	L	L							
lout	L	L	L	L	-----	L	H	H	H							
OUTPUT OF SHIFT REDUNDANCY FUSE CIRCUIT UNIT	H	H	L	H	-----	L	H	H	H							
	↑	↑	↑	↑		↑	↑	↑	↑							
	fj0	f0	f1	f2		f61	f62	f63	fj1							



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Fig. 6

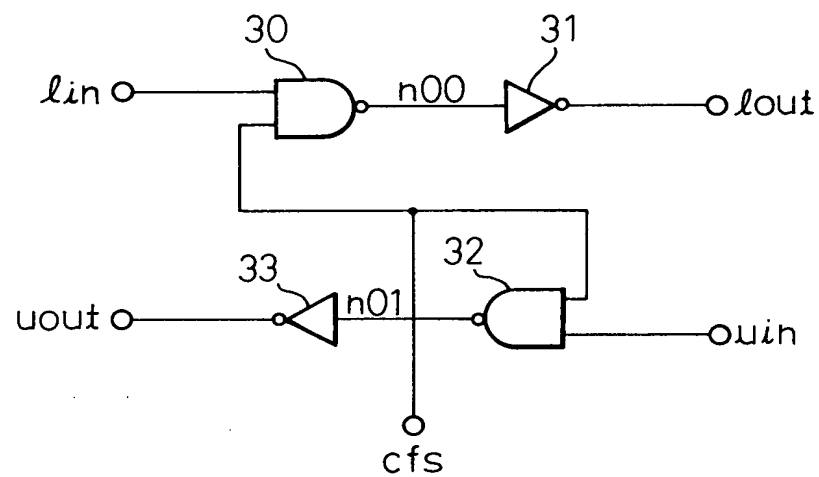




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Fig.7

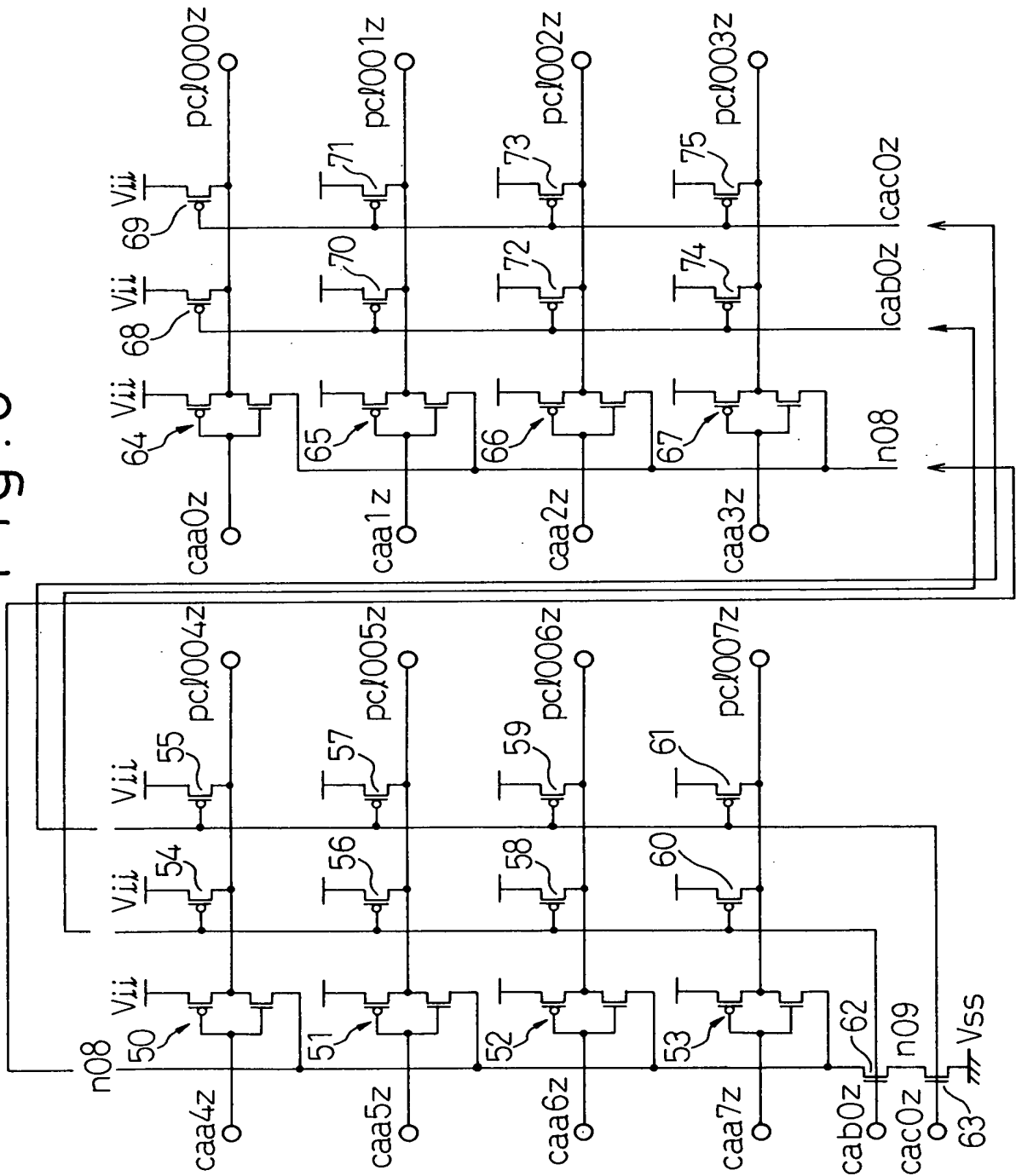




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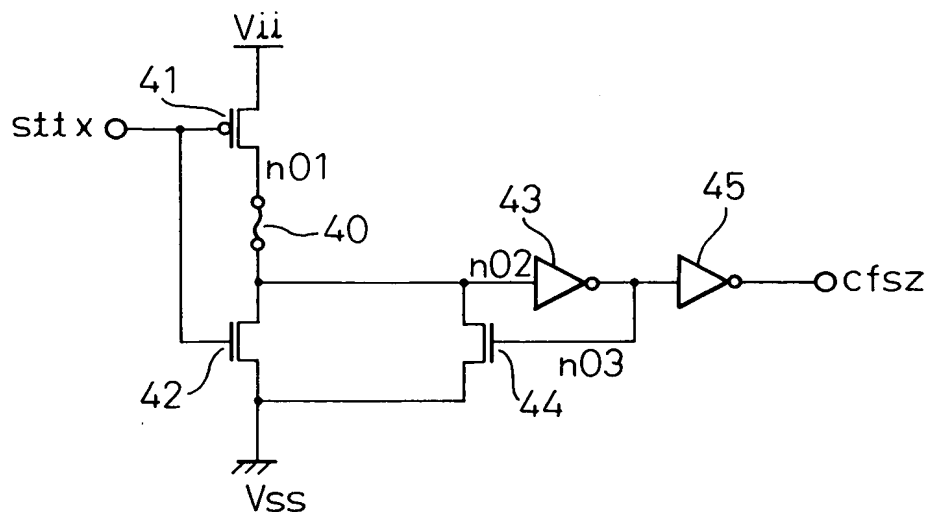
Fig. 8





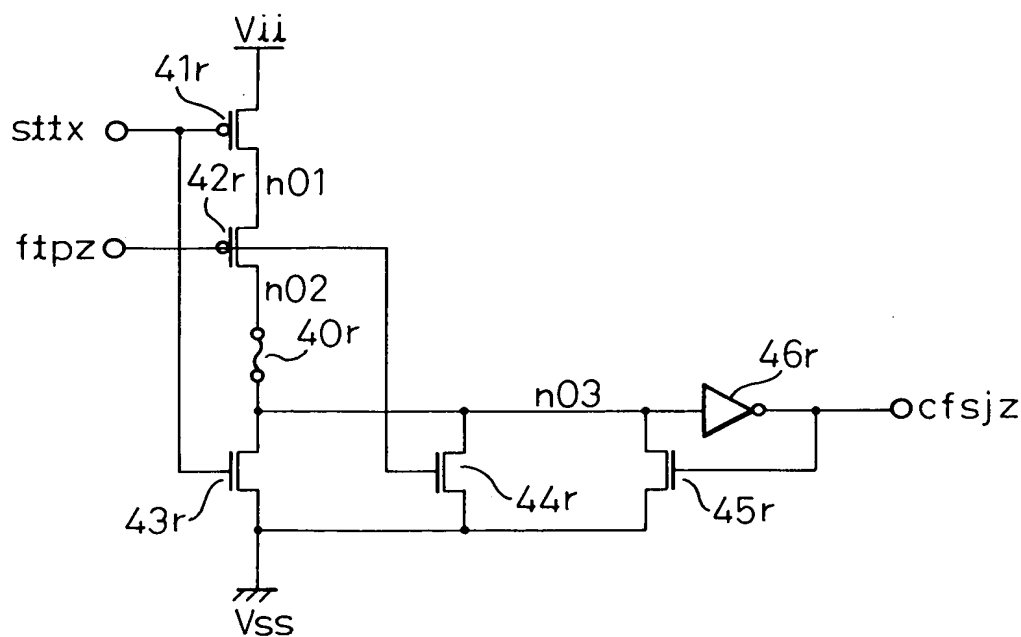
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Fig.9



(USED FOR SELECTING LINES
 cl0,cl2 TO cl61 AND cl63)

Fig.10

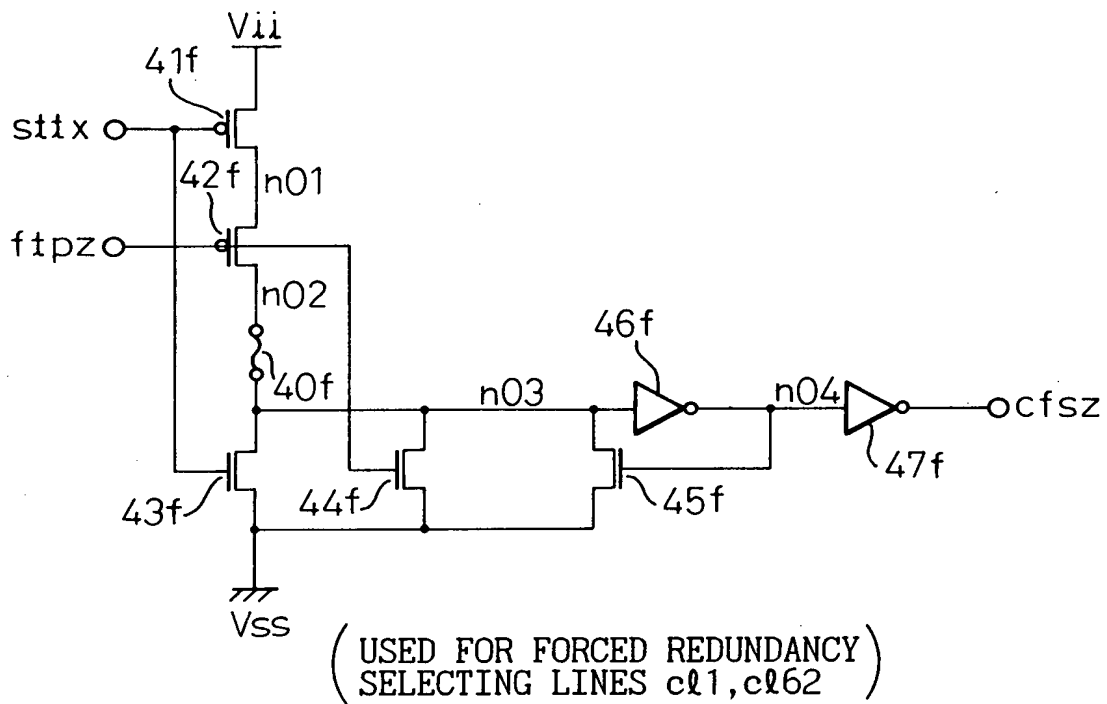


(USED FOR REDUNDANCY
 SELECTING LINES clj0,clj1)



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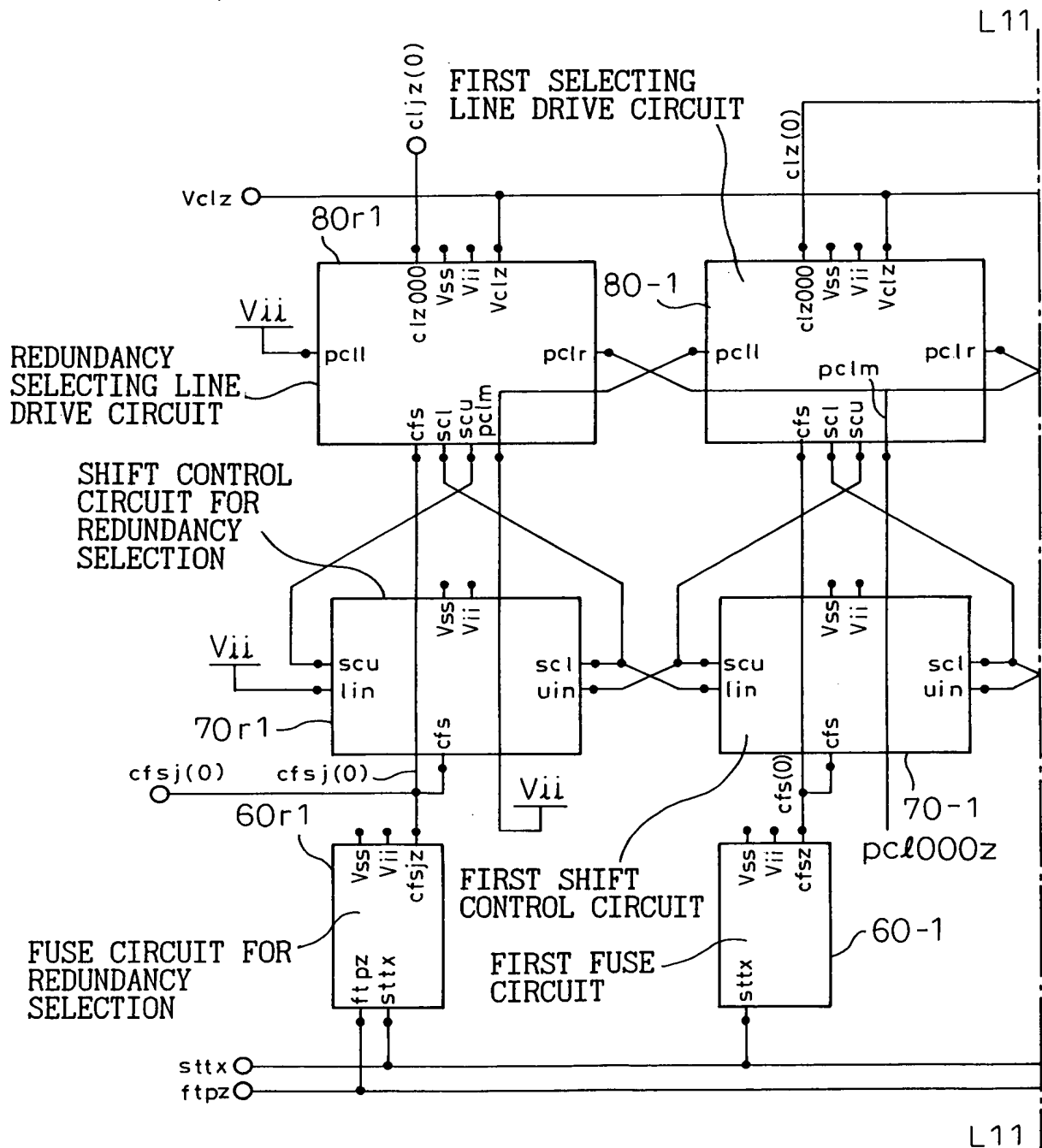
Fig.11





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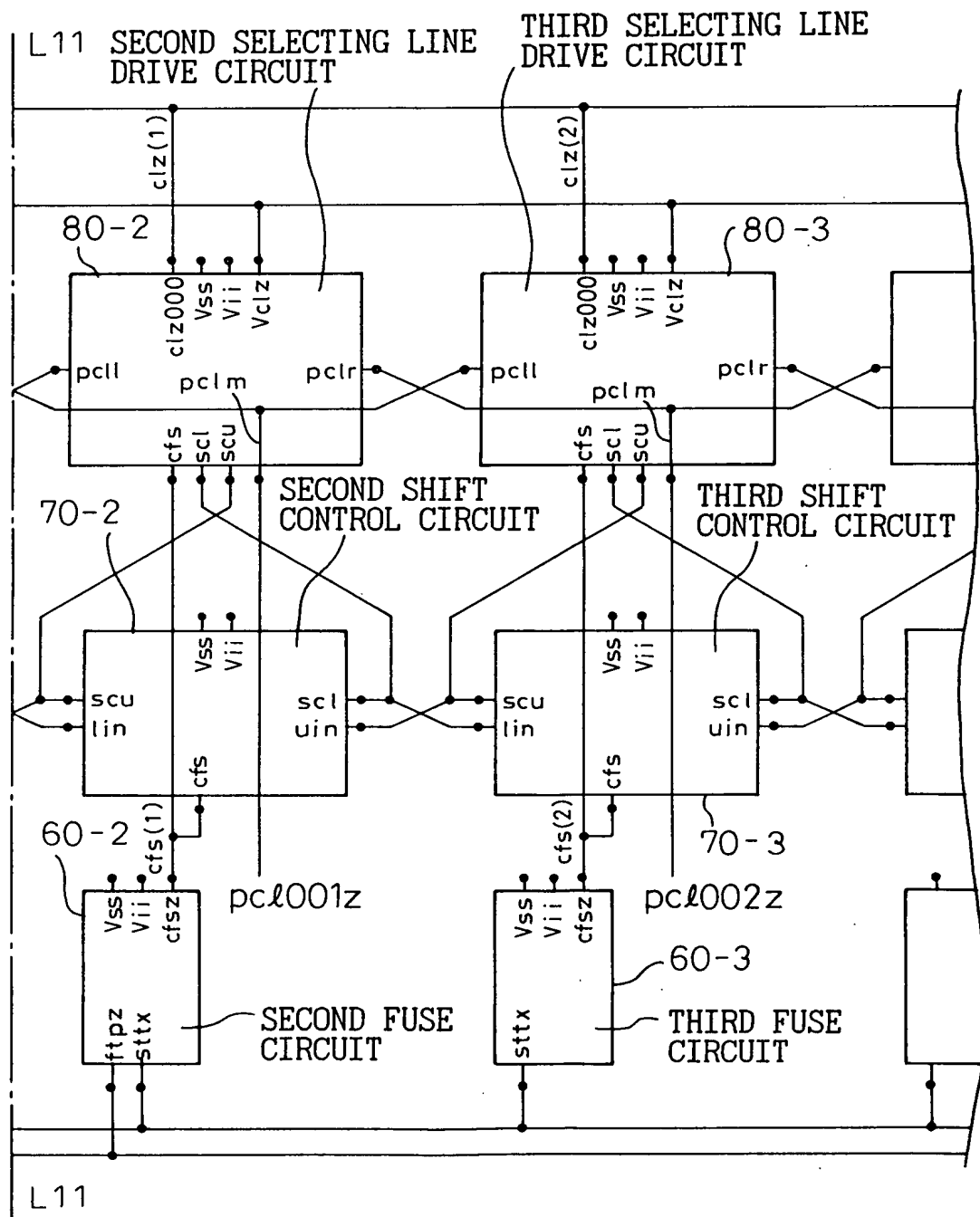
Fig.12





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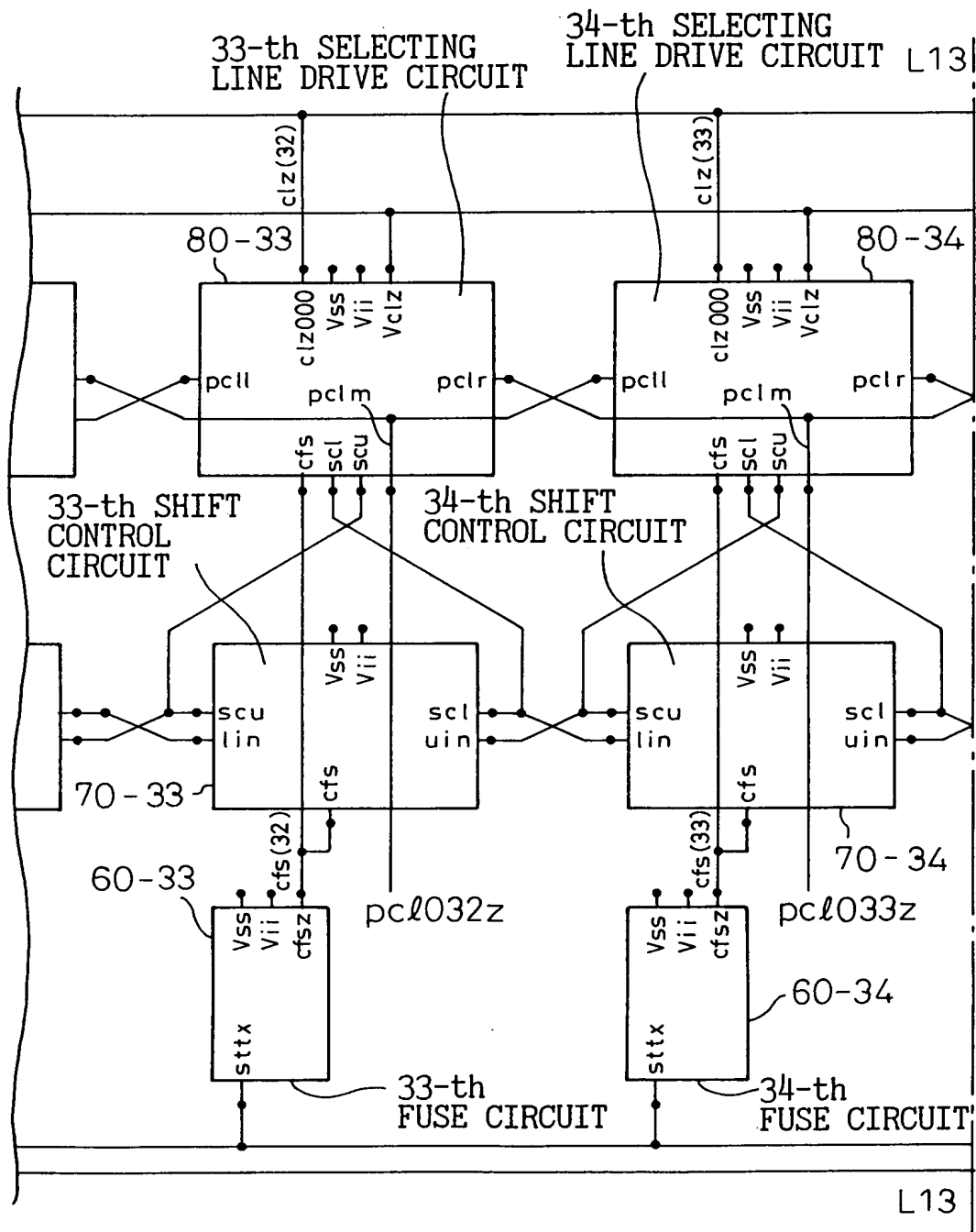
Fig.13





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Fig.14

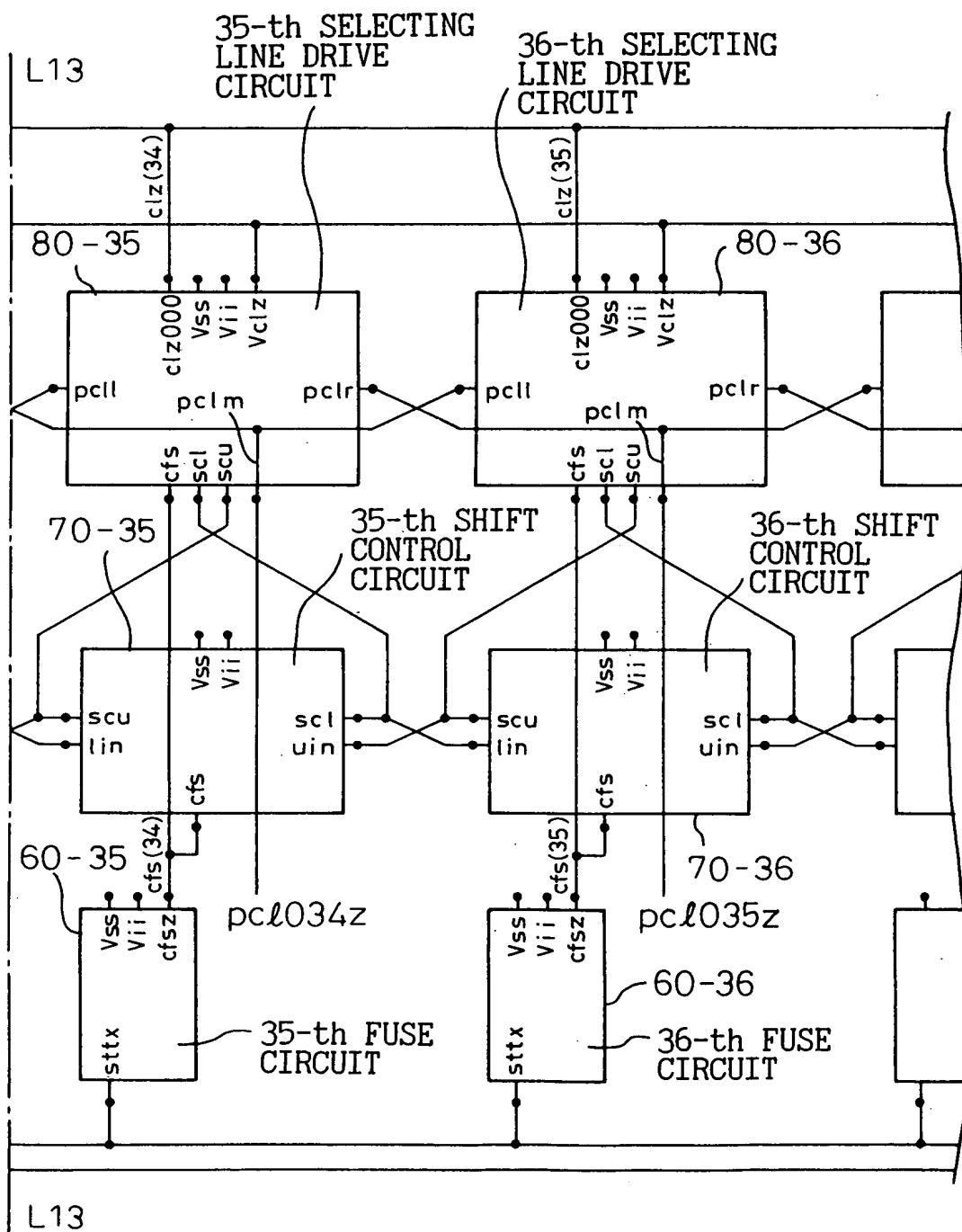


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Fig.15





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Fig.16

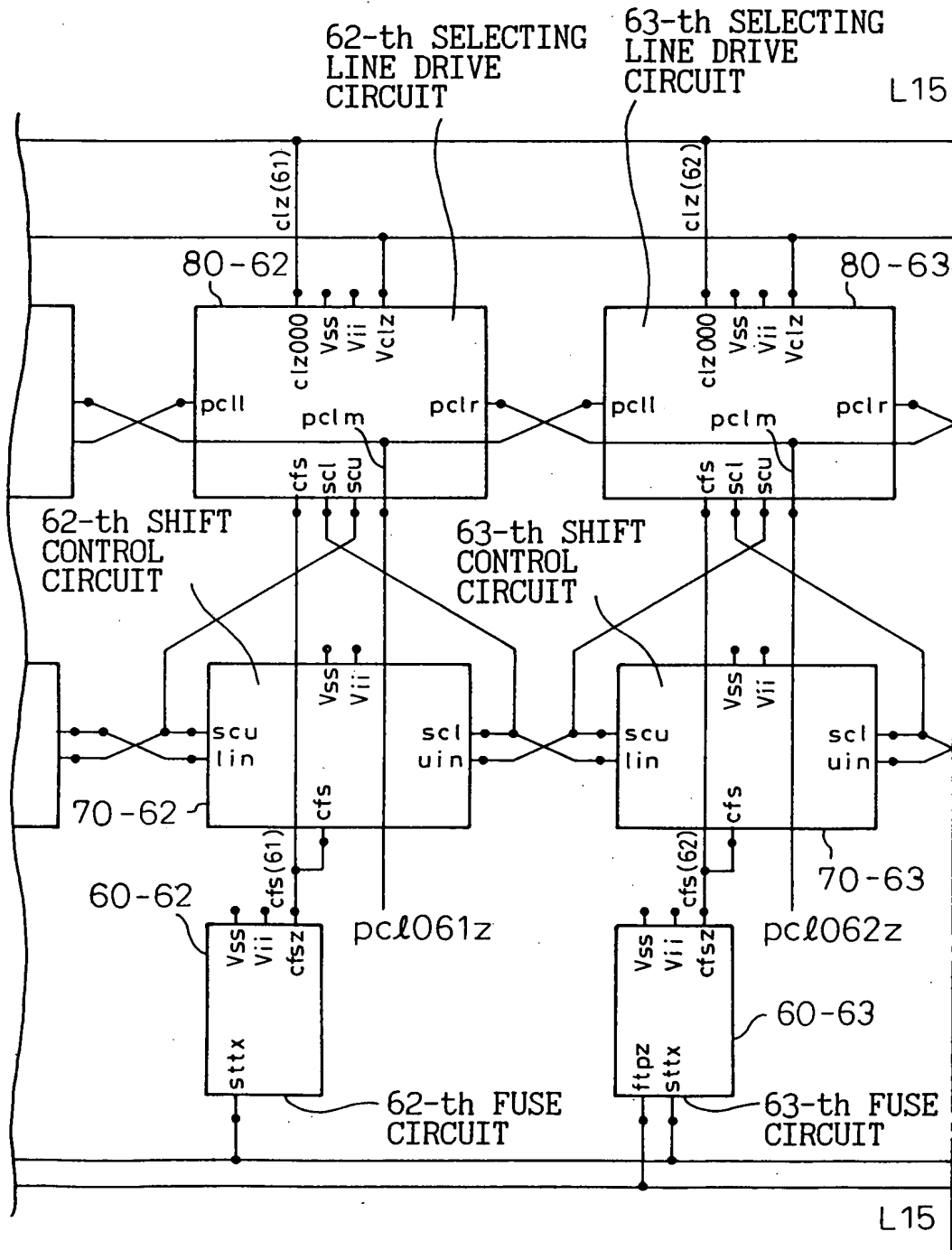
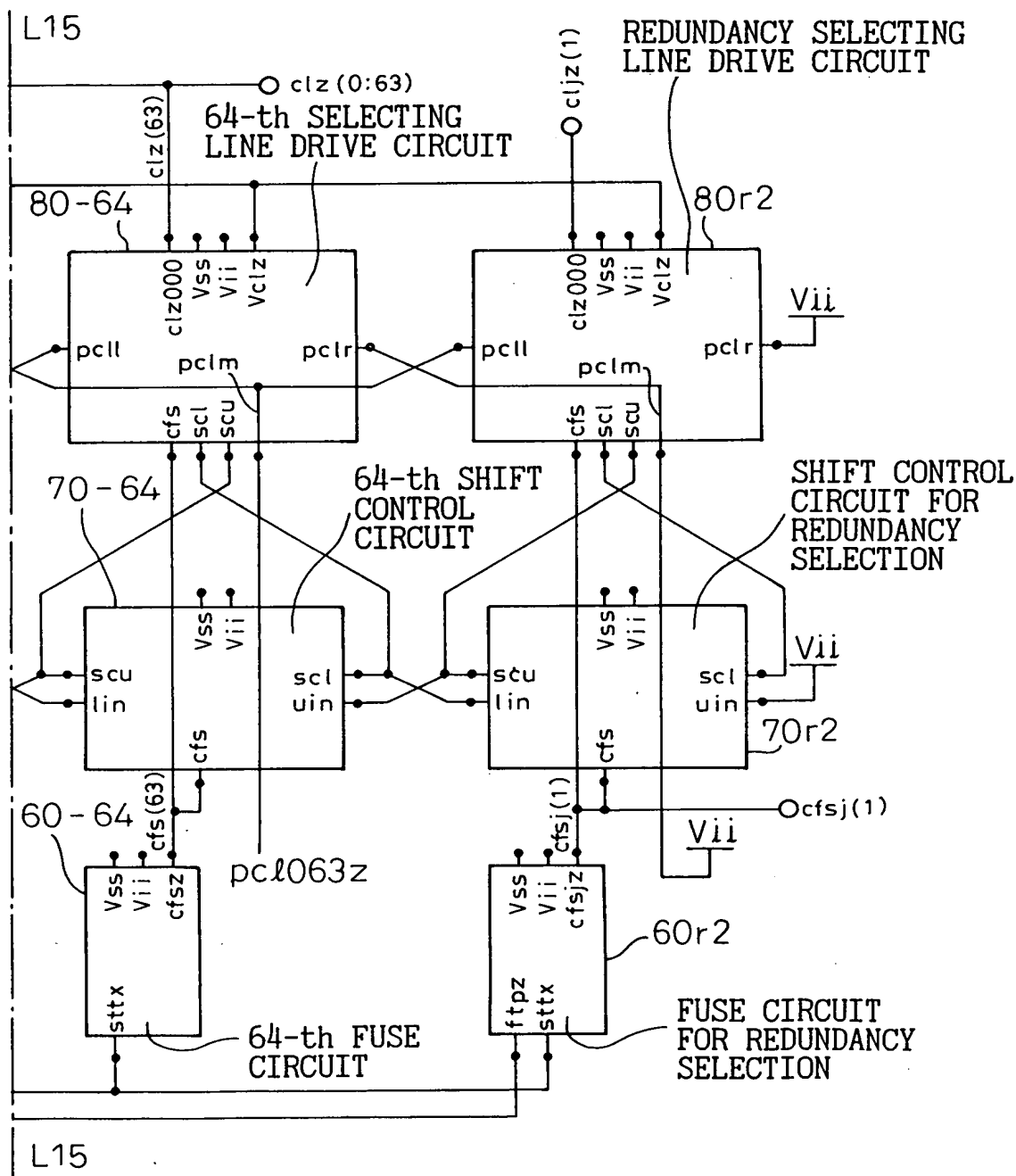




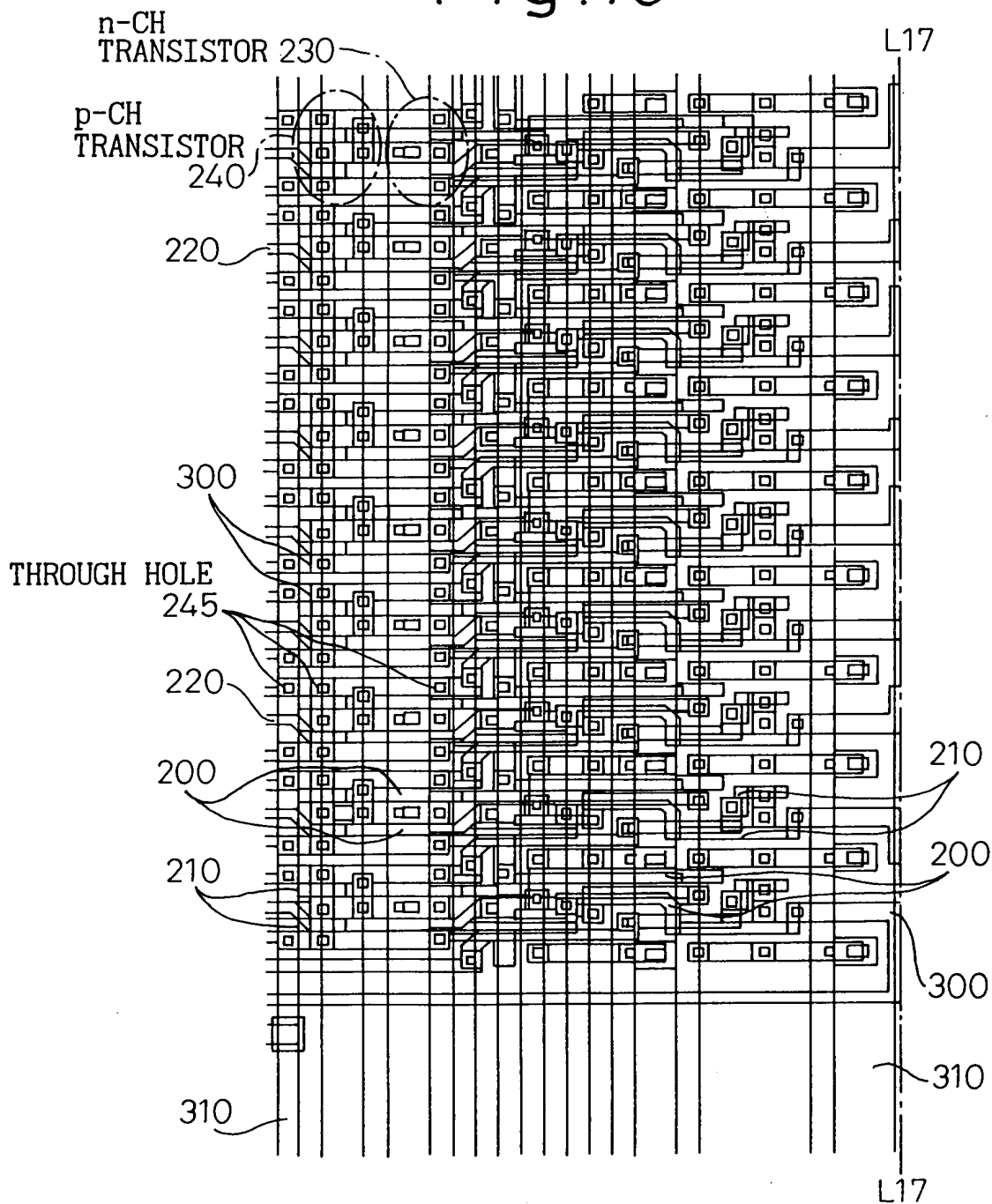
Fig.17





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Fig.18

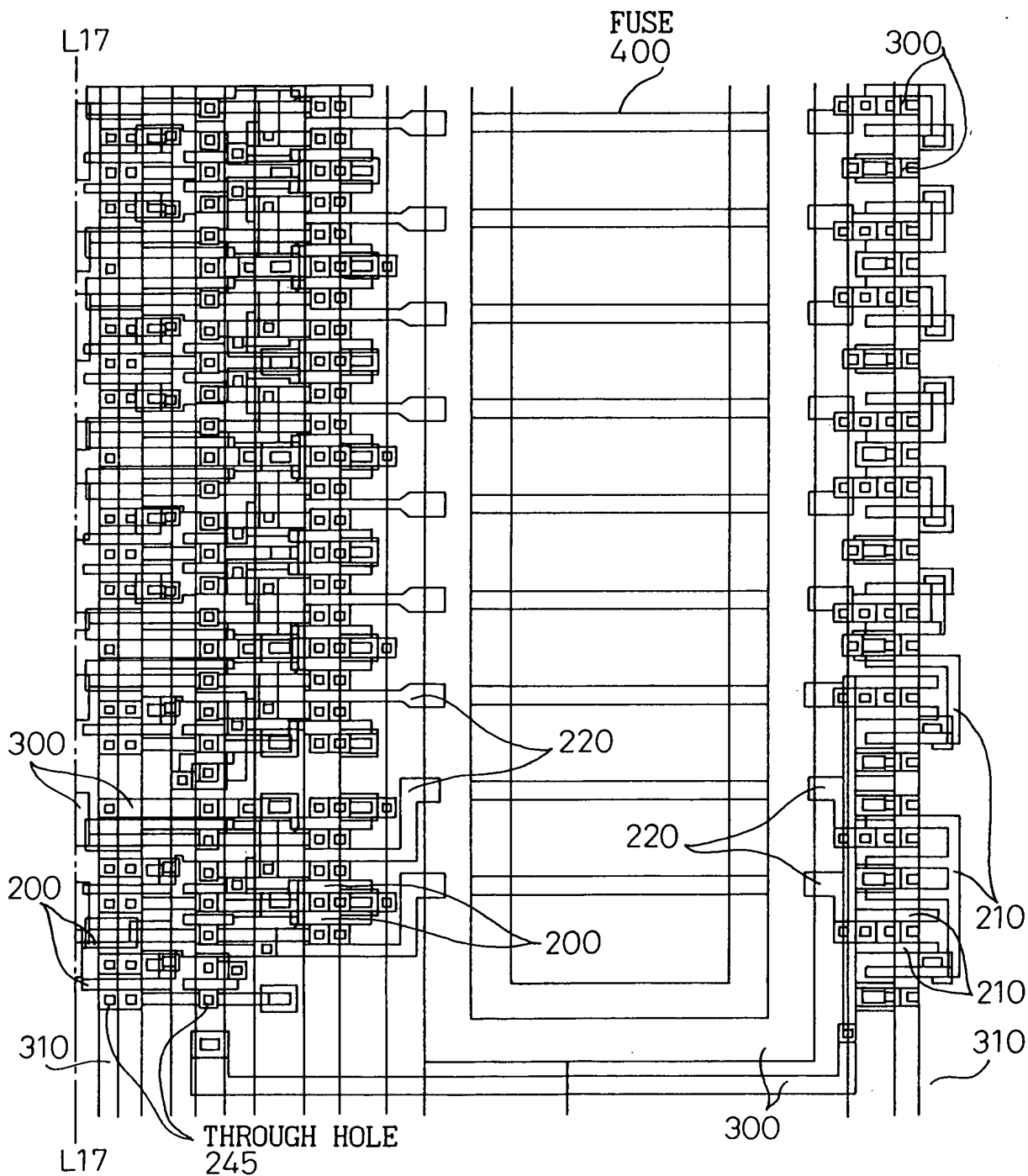




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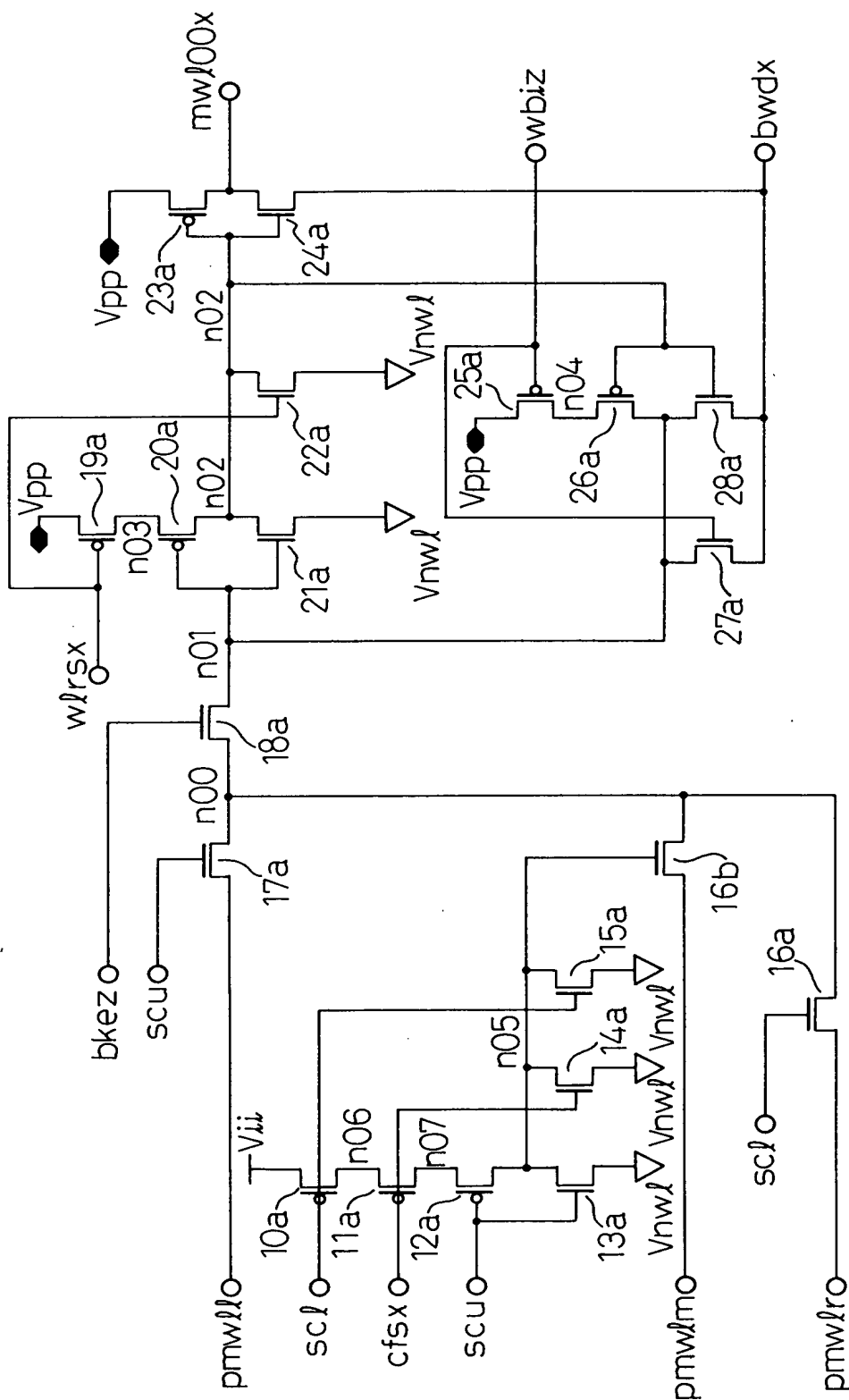
Fig.19





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Fig. 20

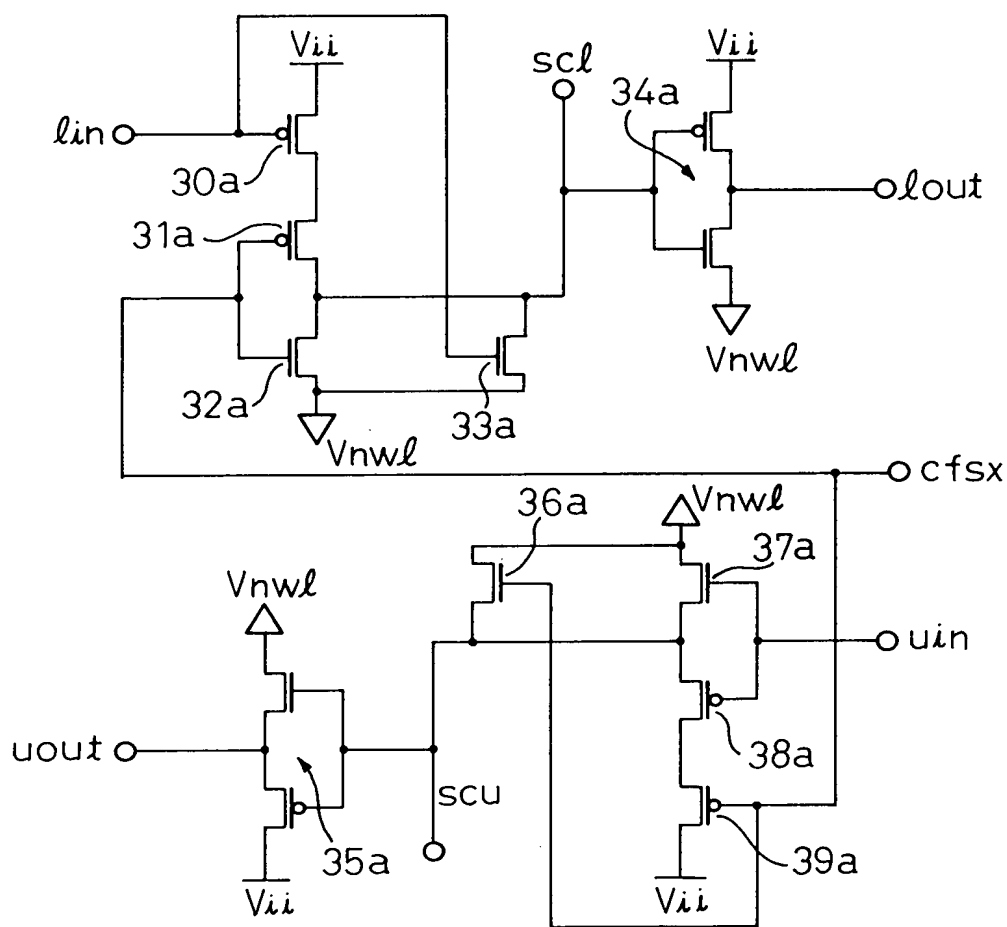




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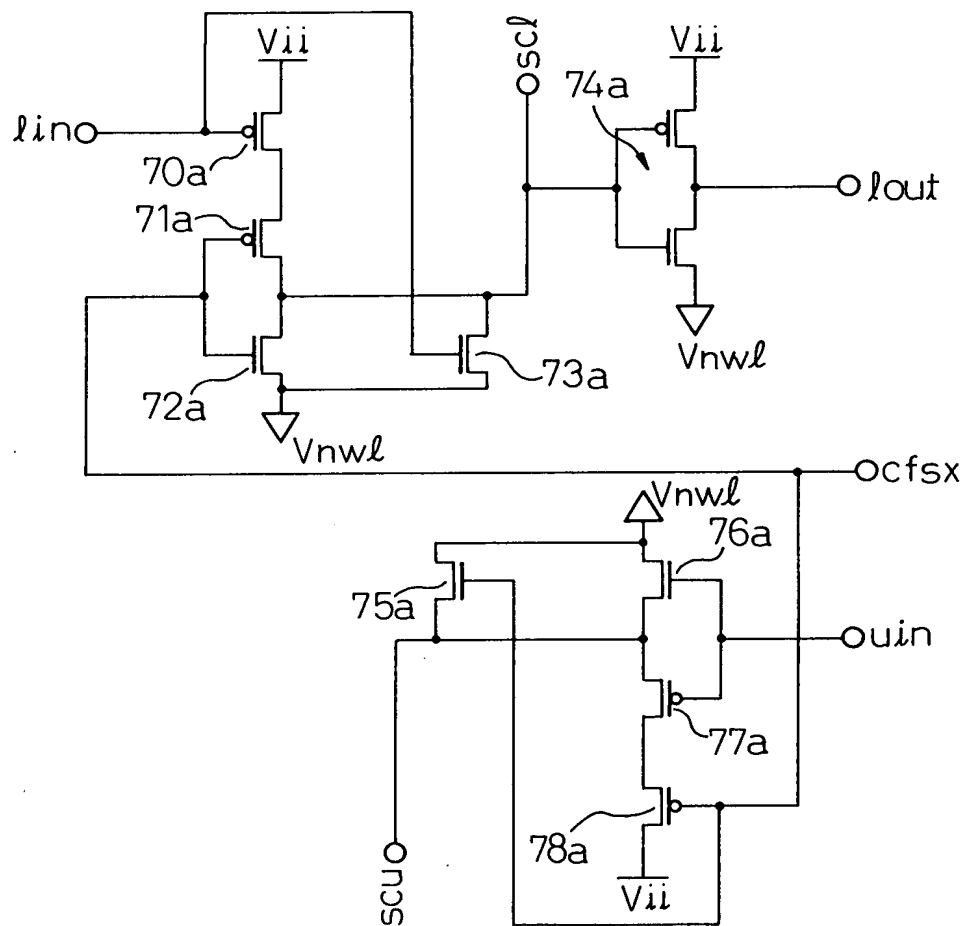
Fig. 21





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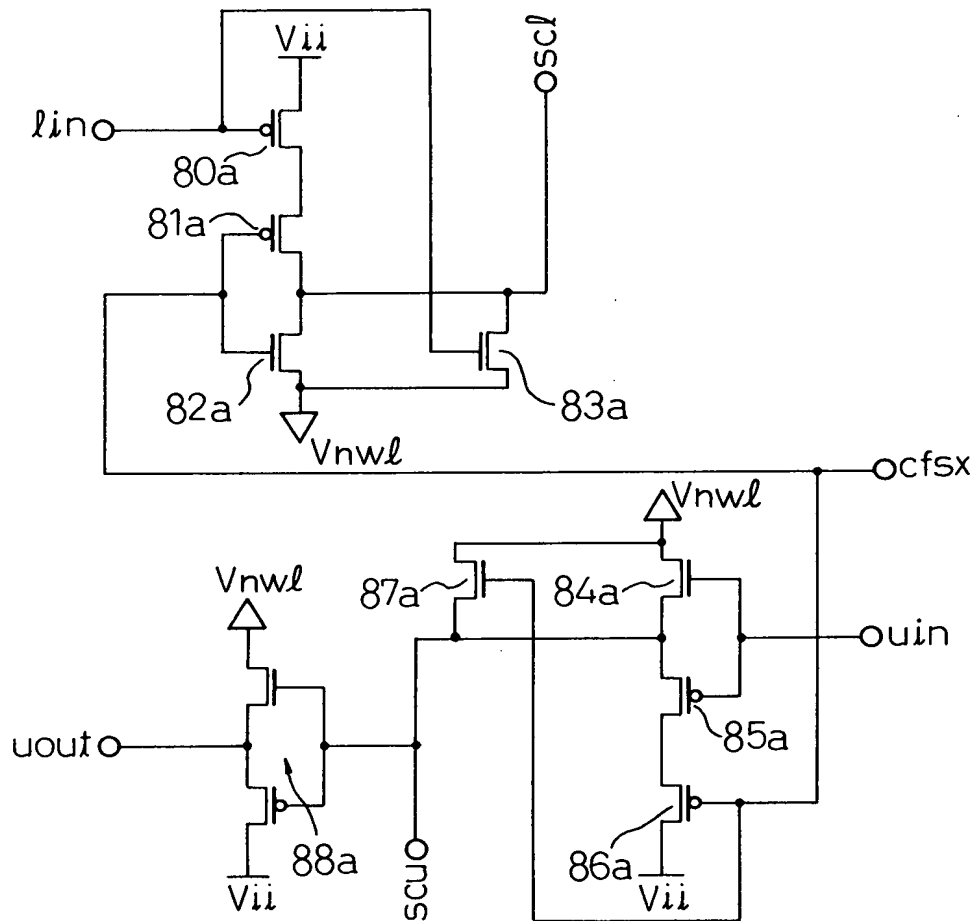
Fig. 22





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Fig. 23





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Fig. 24

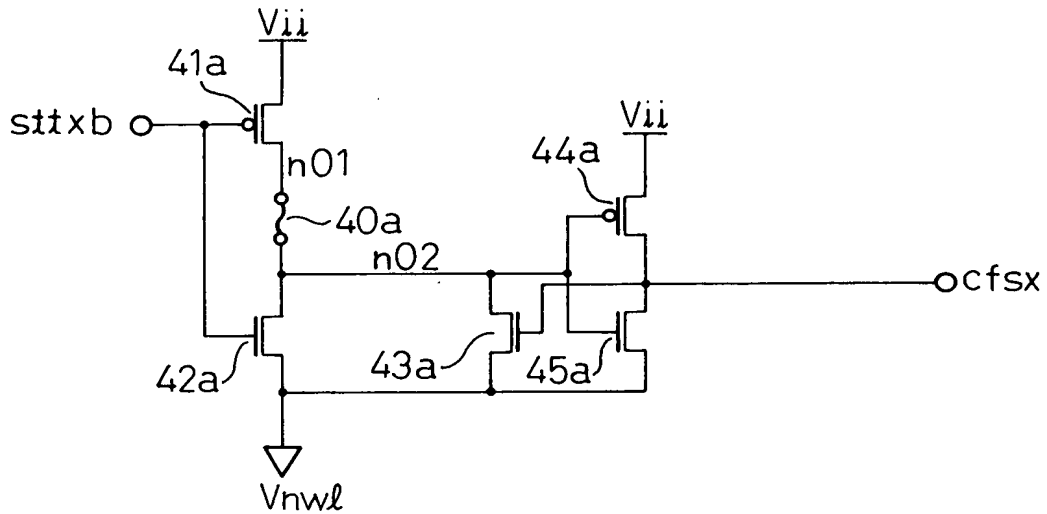
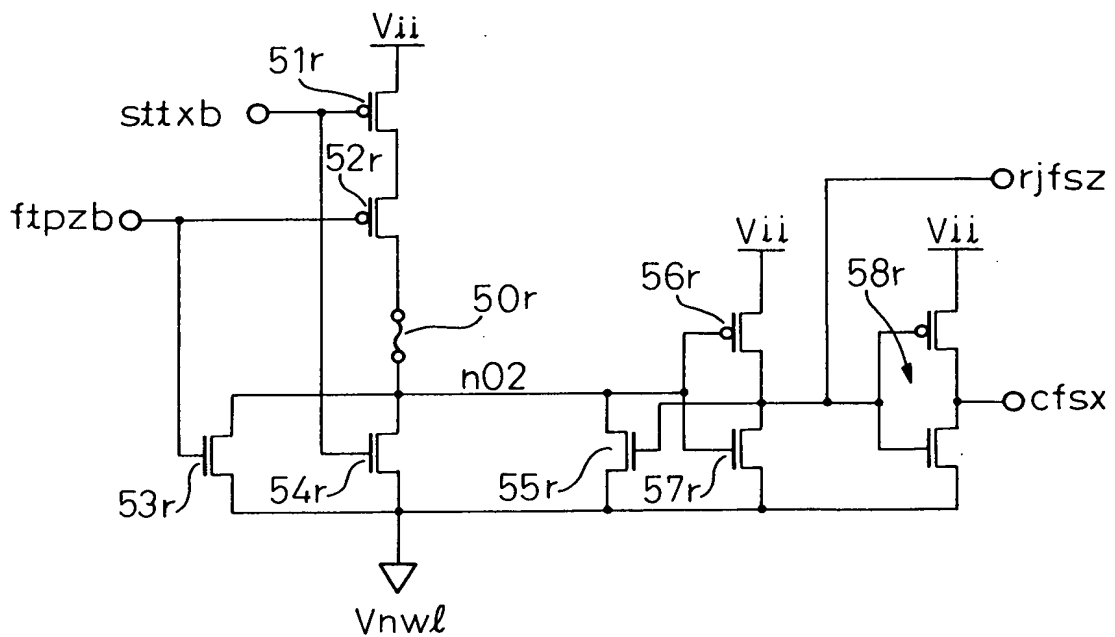


Fig. 25





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Fig.26

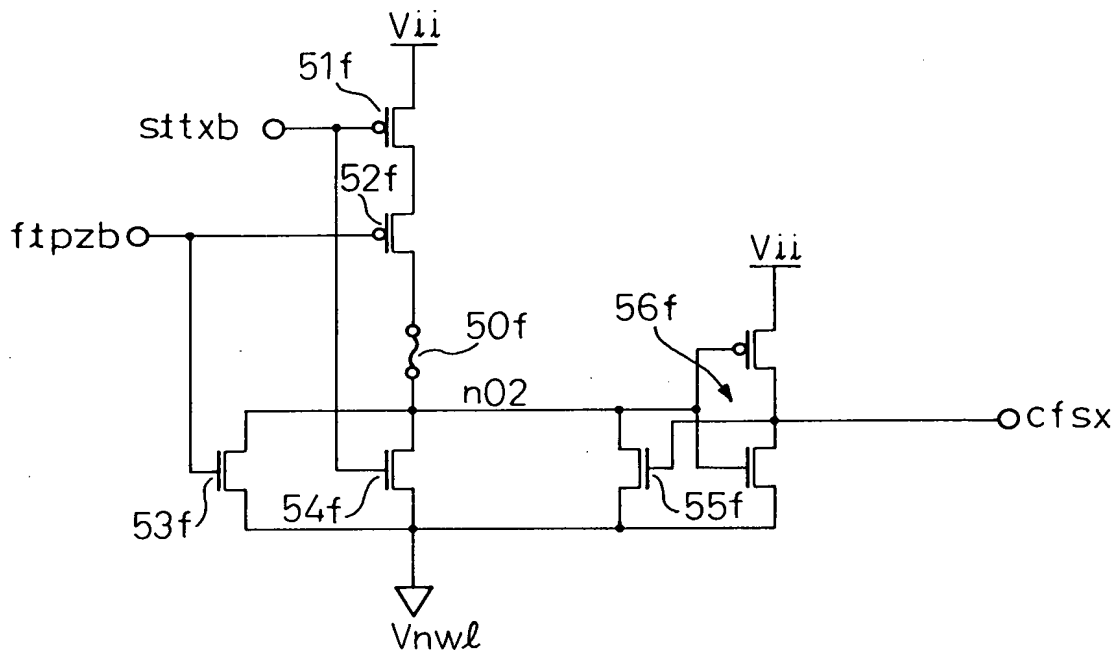
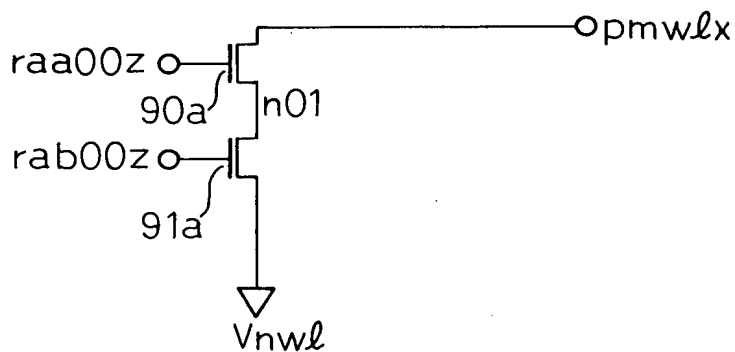


Fig.27





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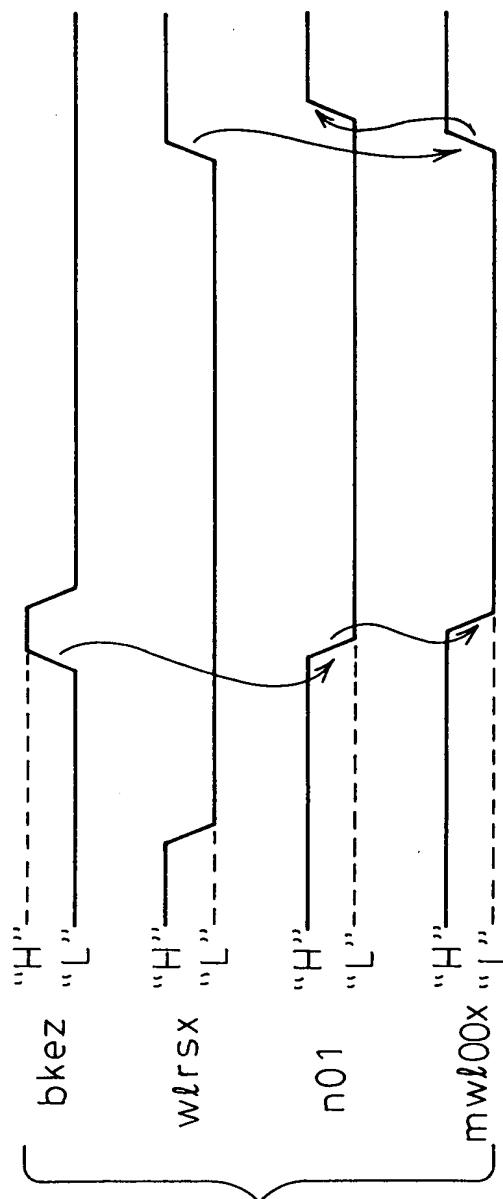


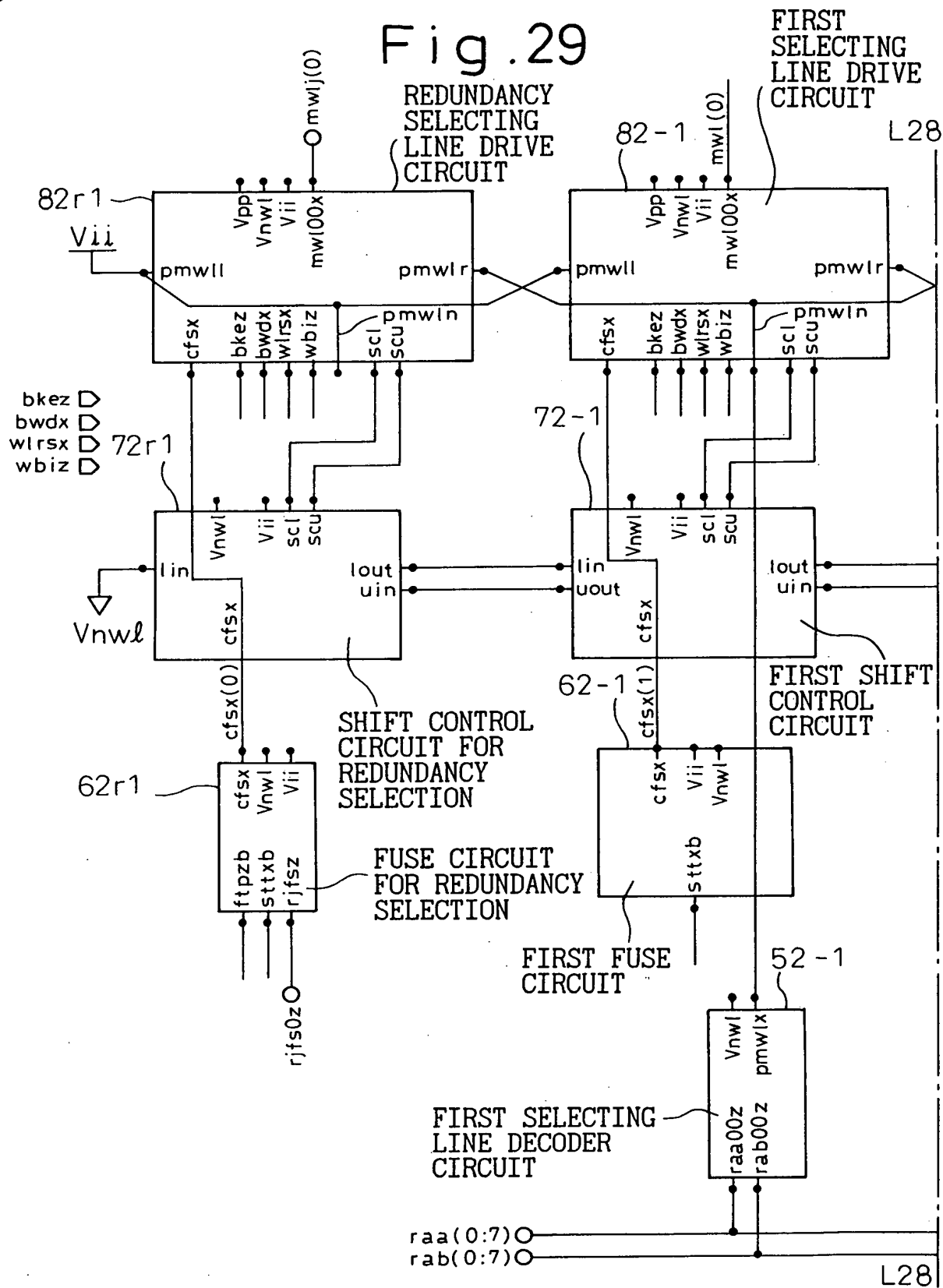
Fig. 28

wb1z="L"
 bwdx="L"



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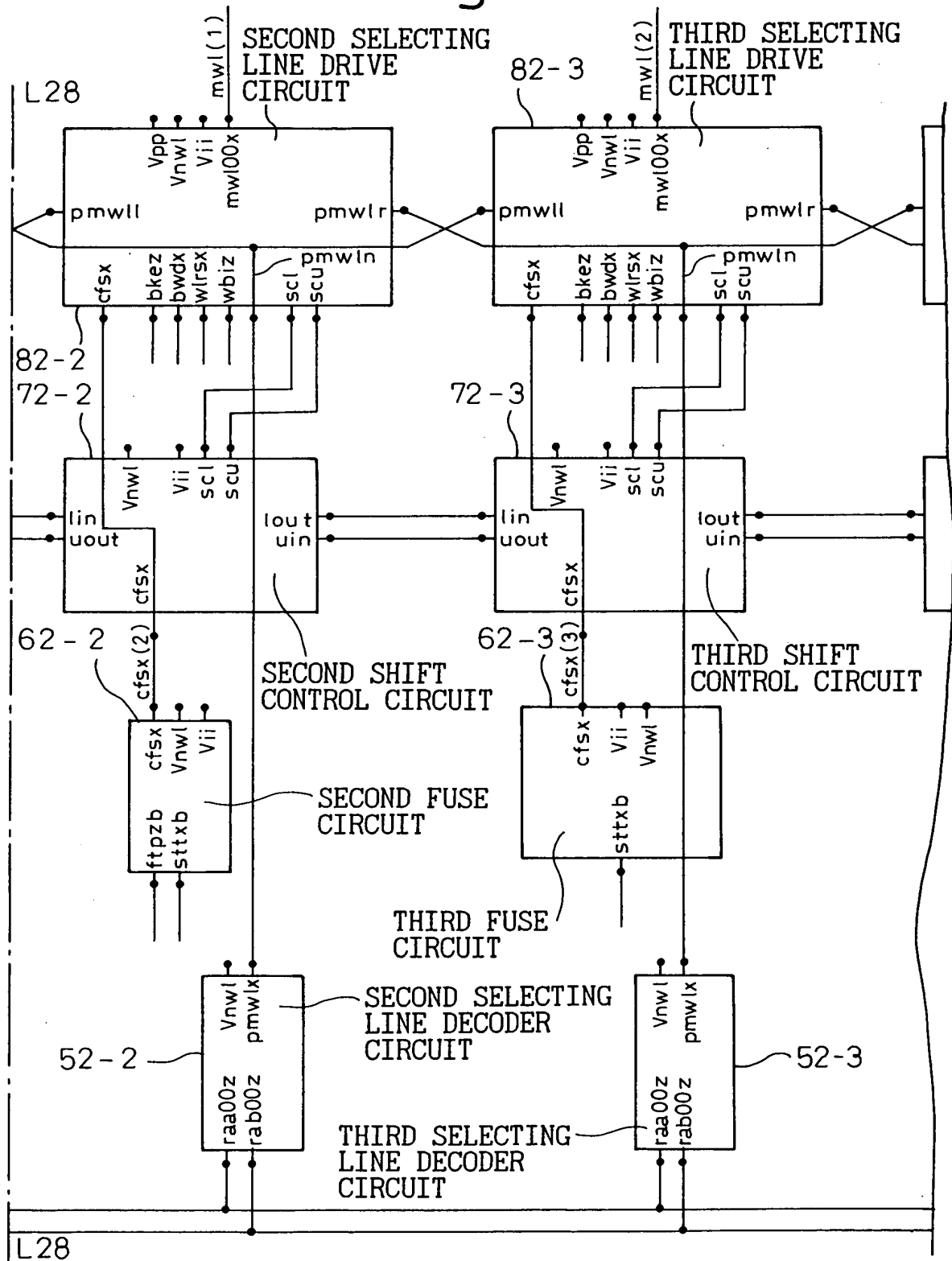
Fig. 29

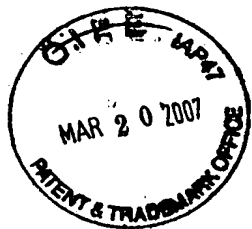




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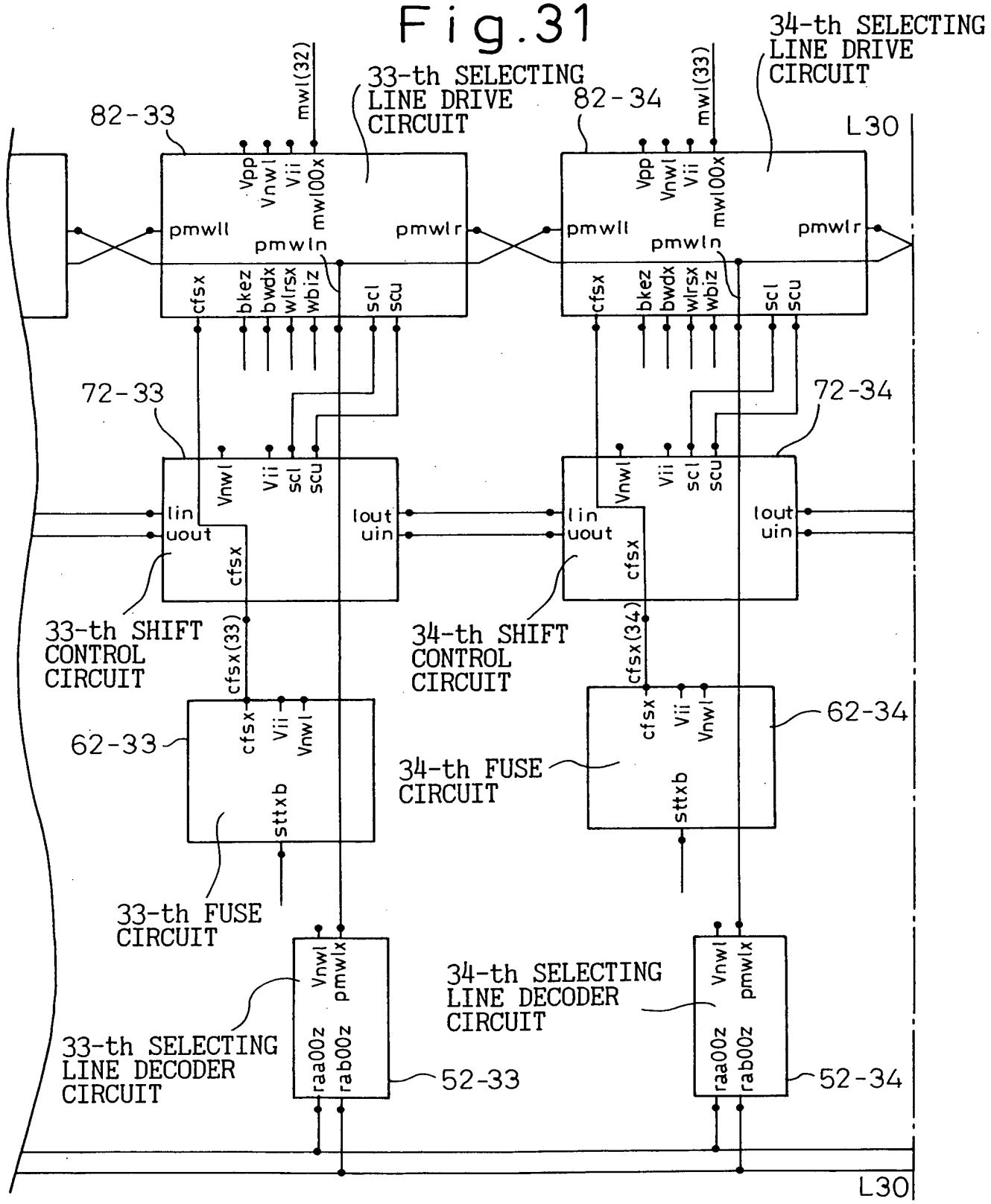
Fig. 30

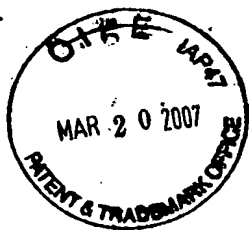




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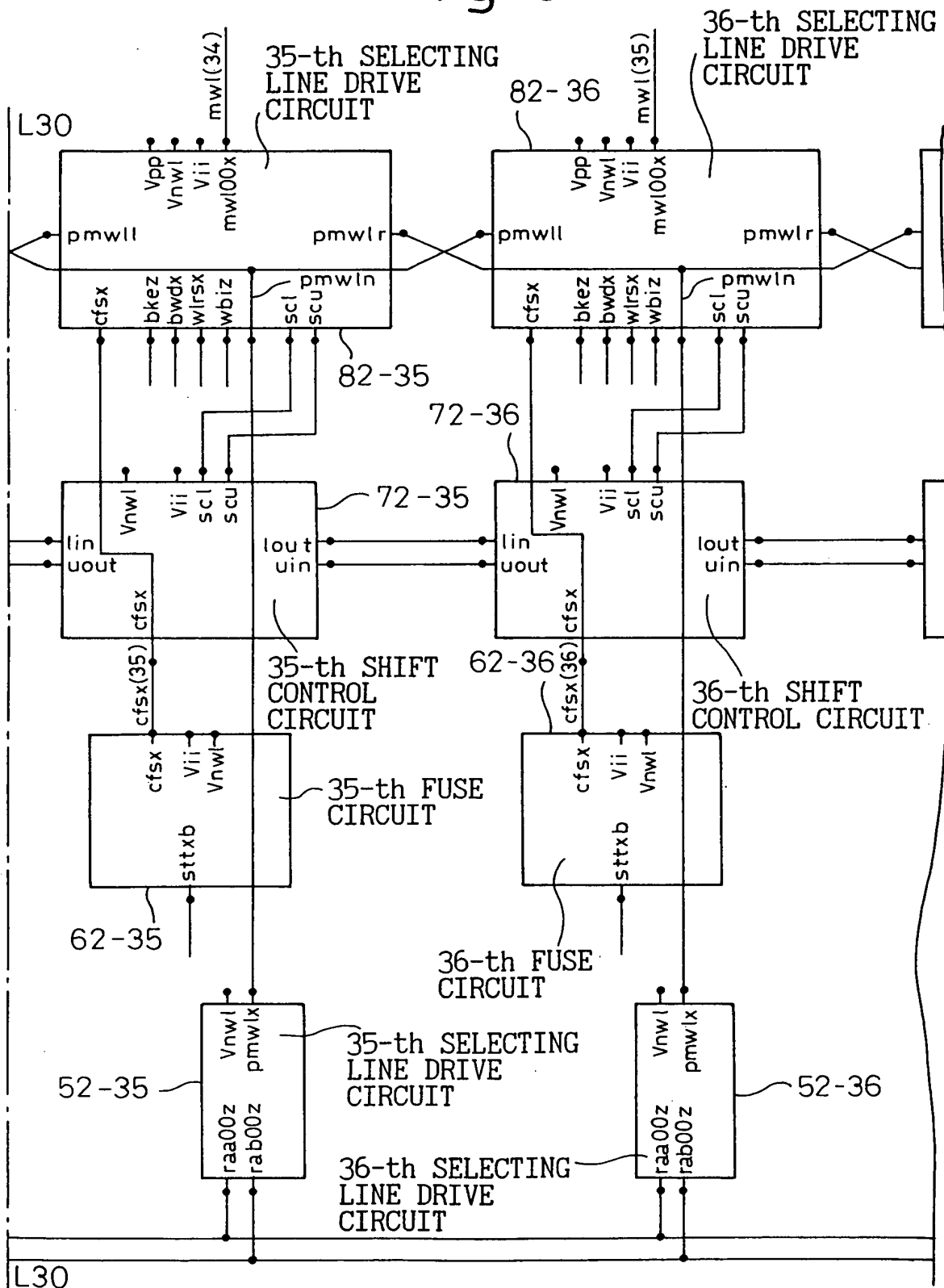
Fig.31





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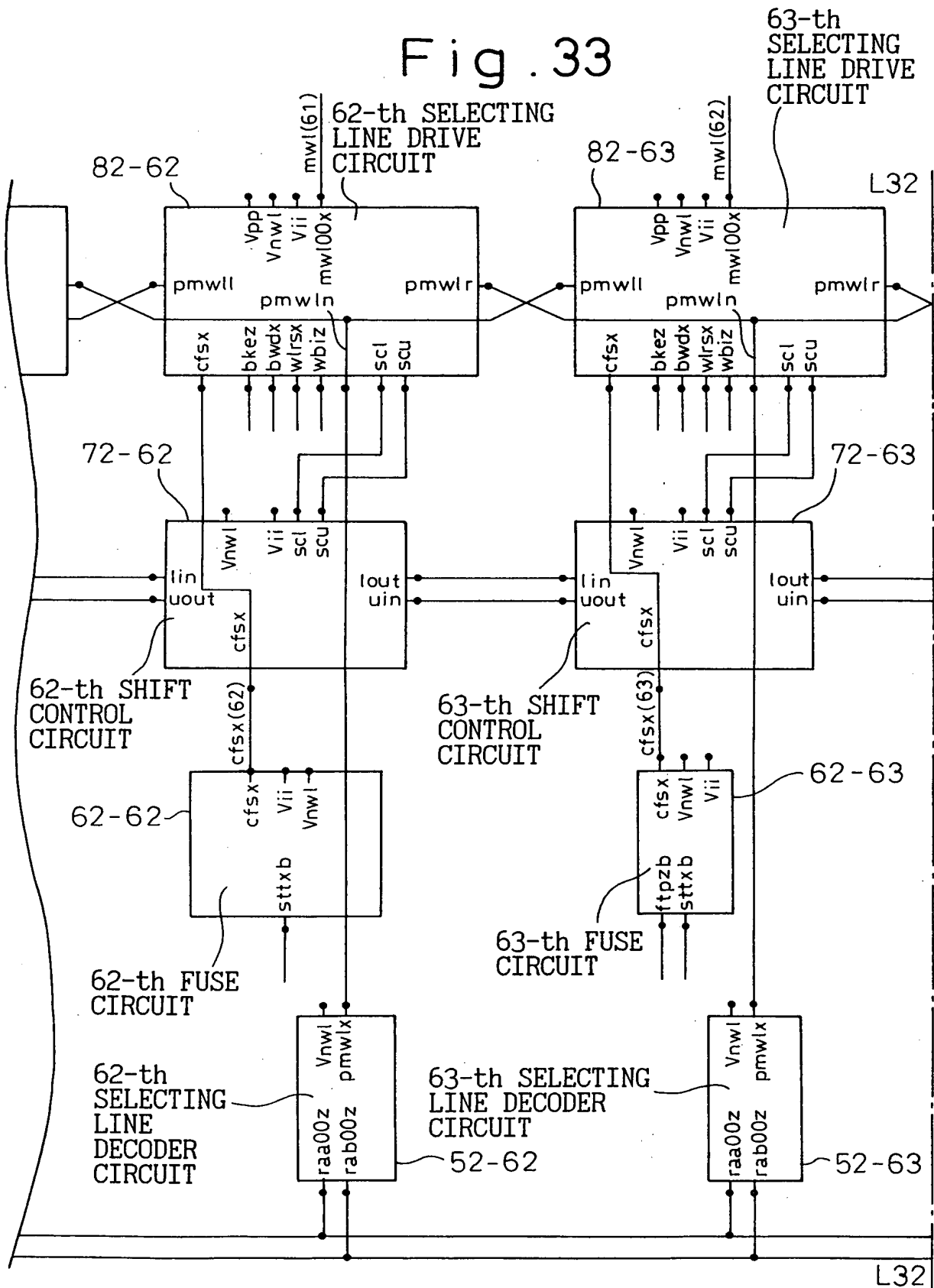
Fig.32





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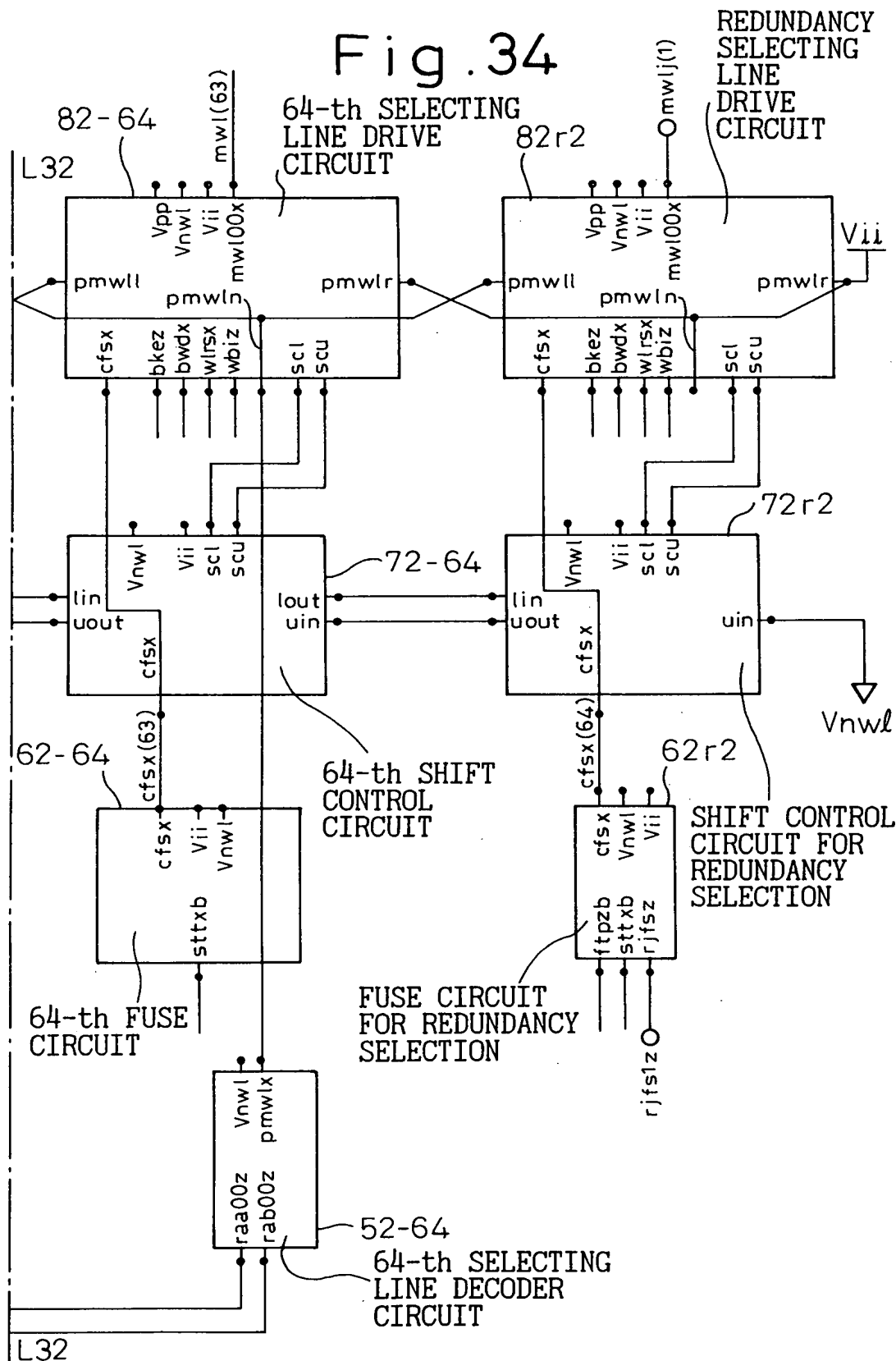
Fig. 33





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Fig. 34





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Fig. 35

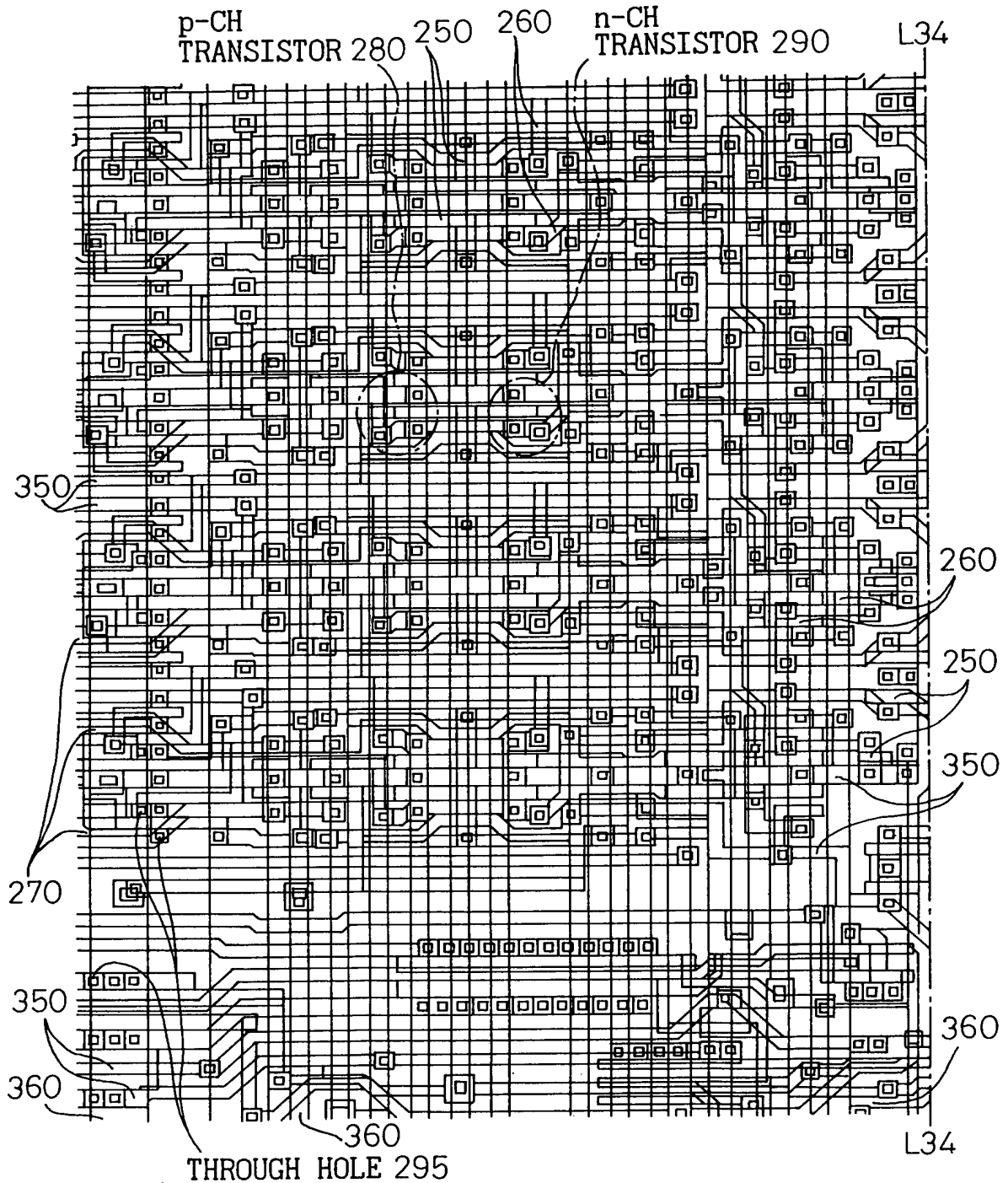




Fig.36

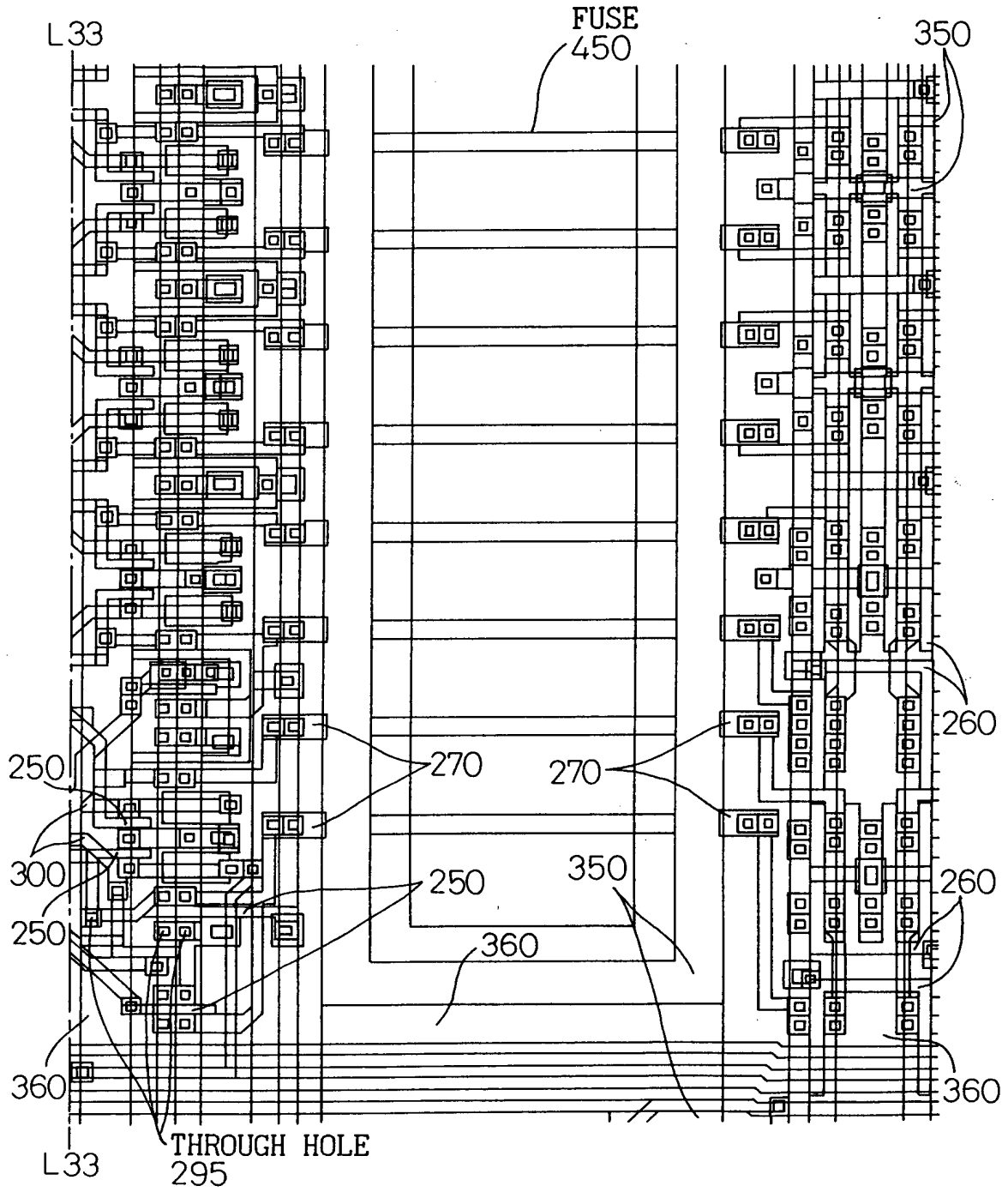
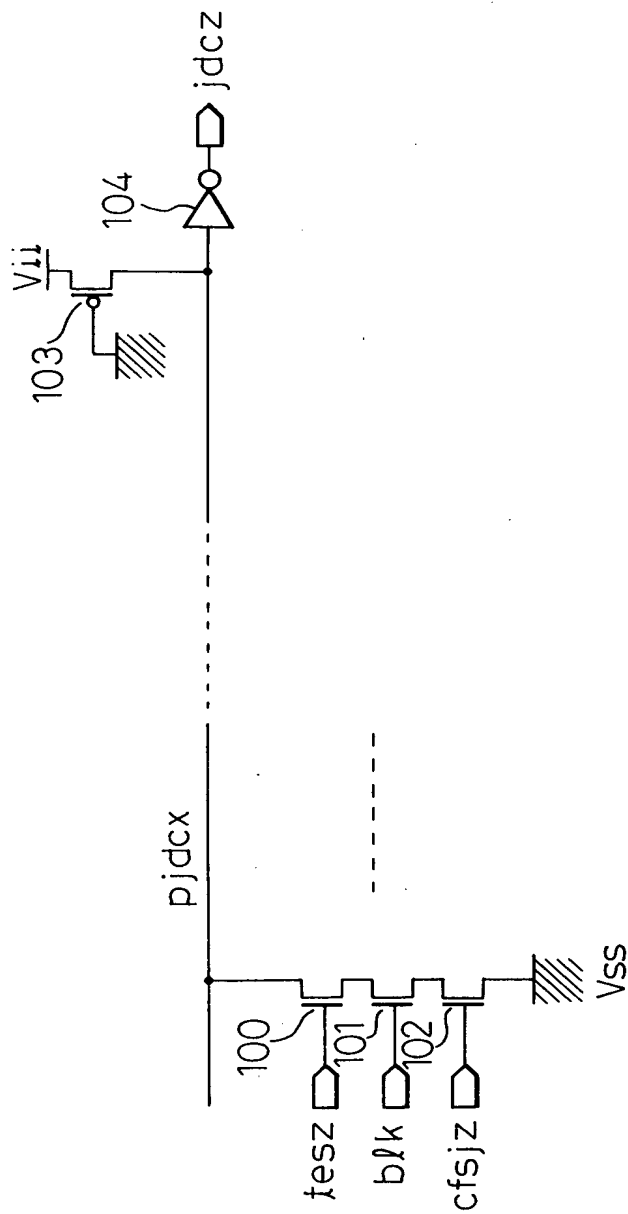


Fig. 37

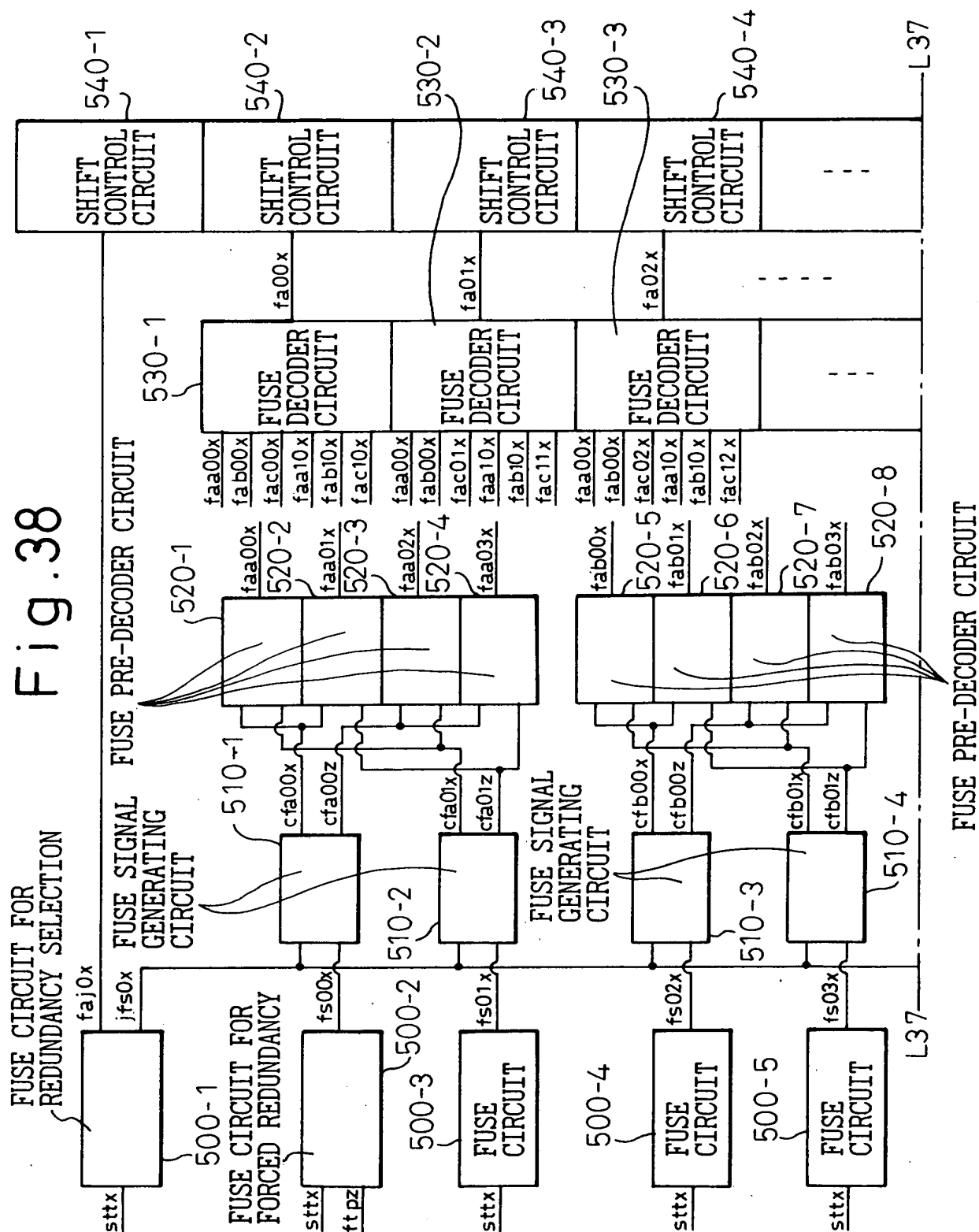


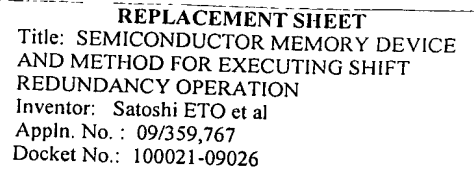
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Fi. 38







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Fig. 41

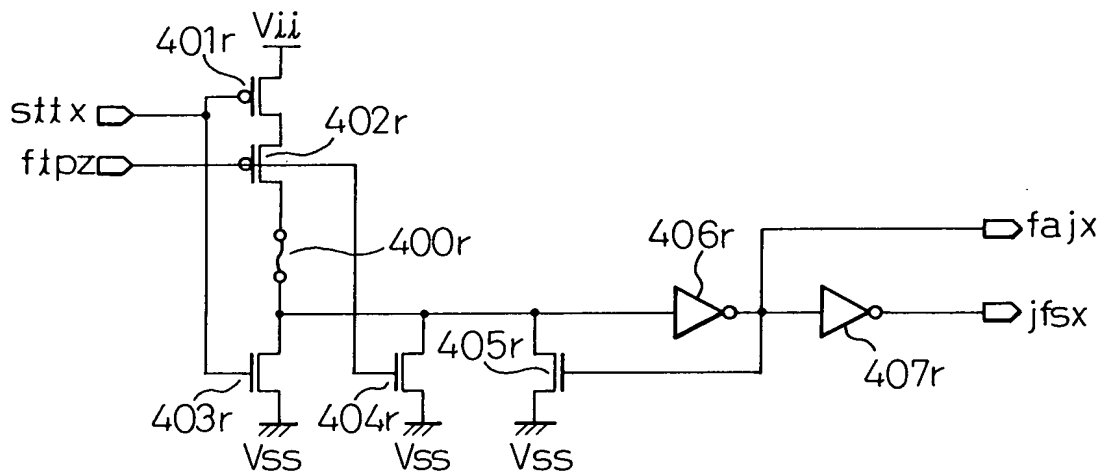
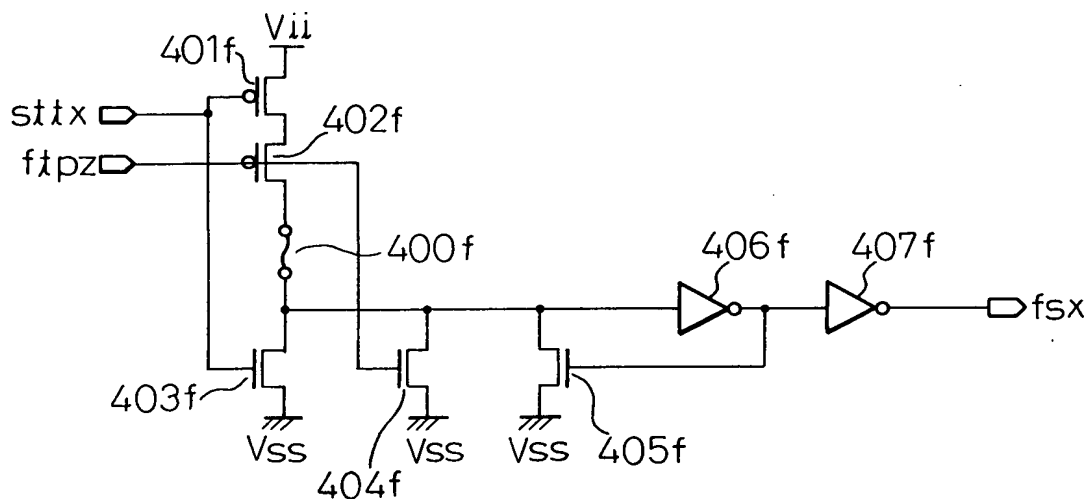


Fig. 42





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Fig. 43

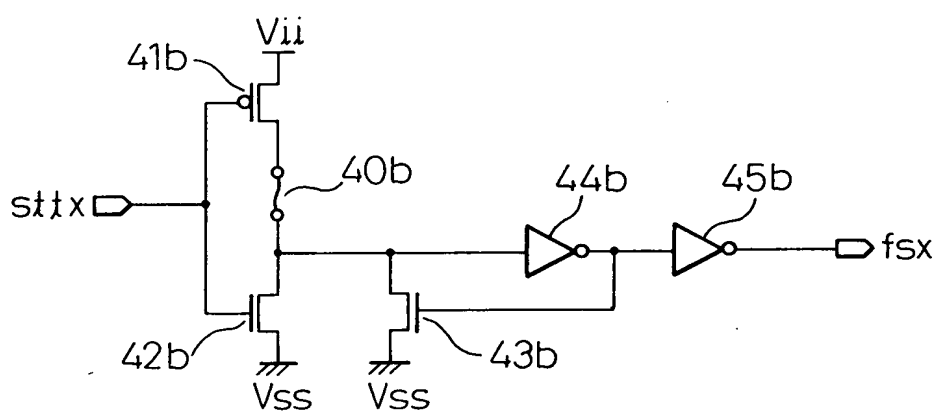


Fig. 44

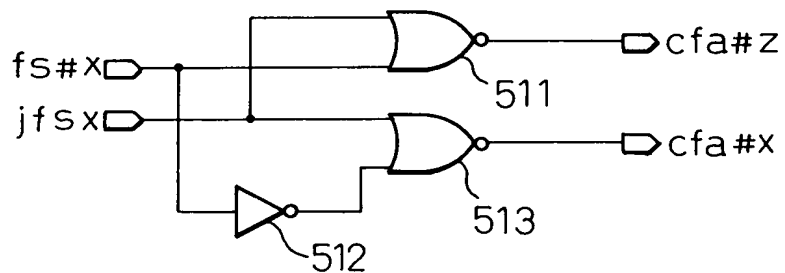




Fig. 45

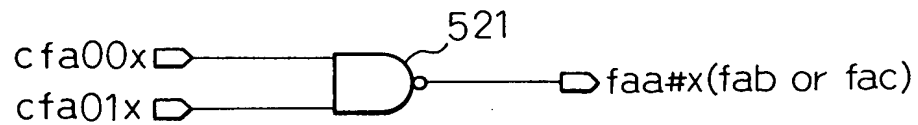
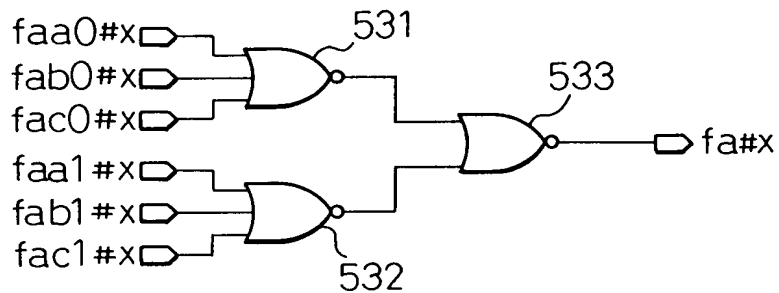


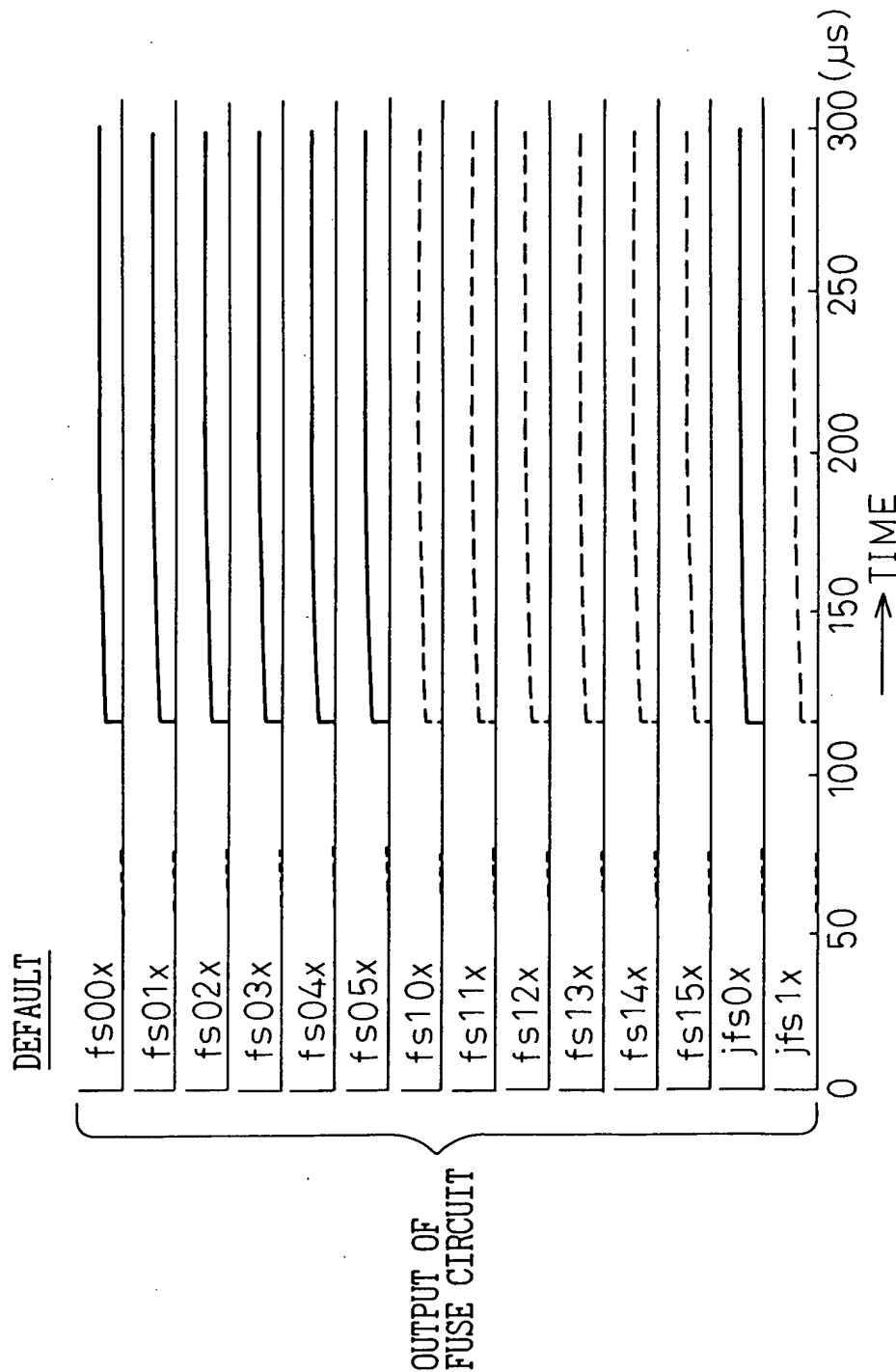
Fig. 46





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Fig. 47

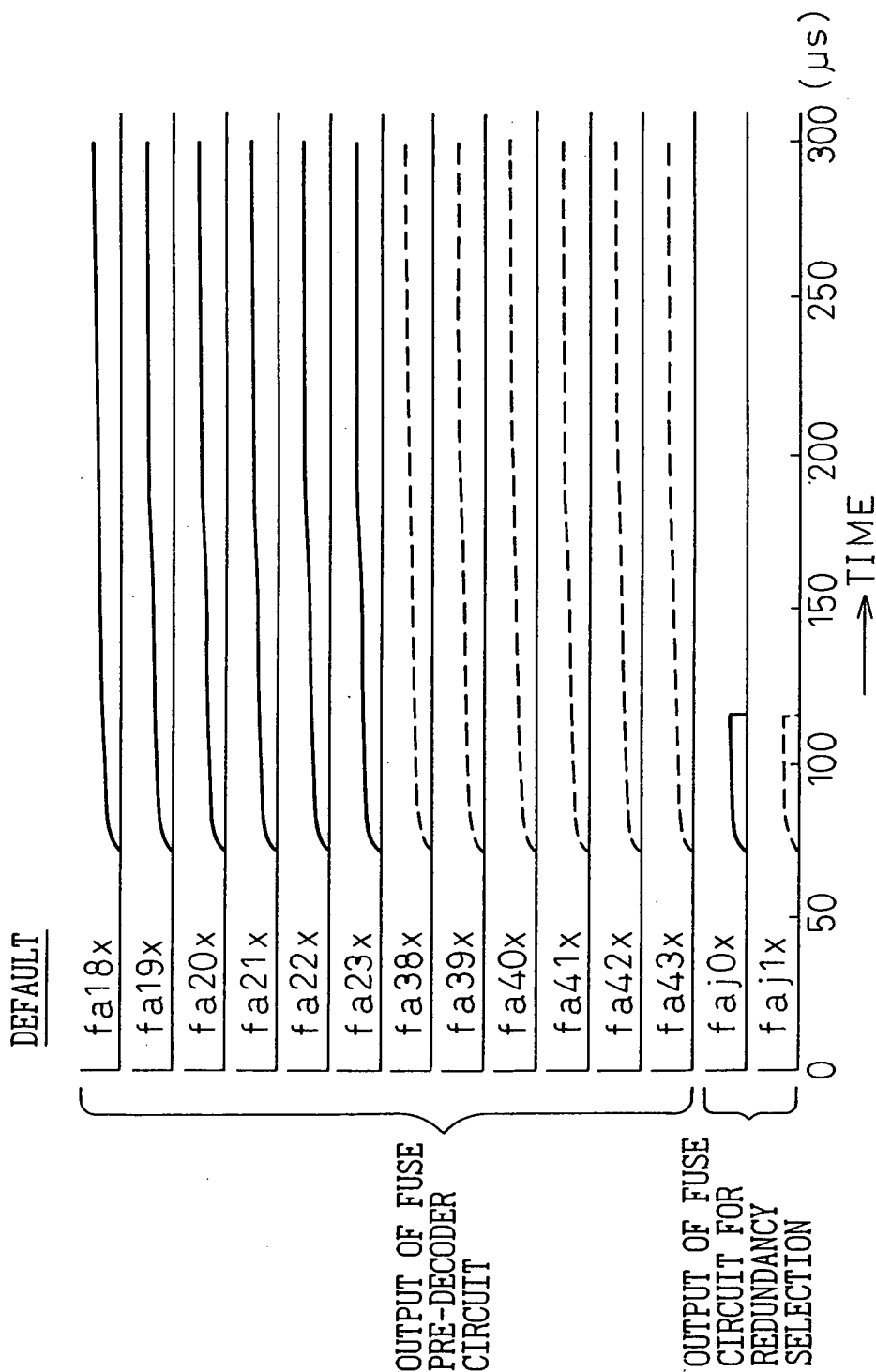




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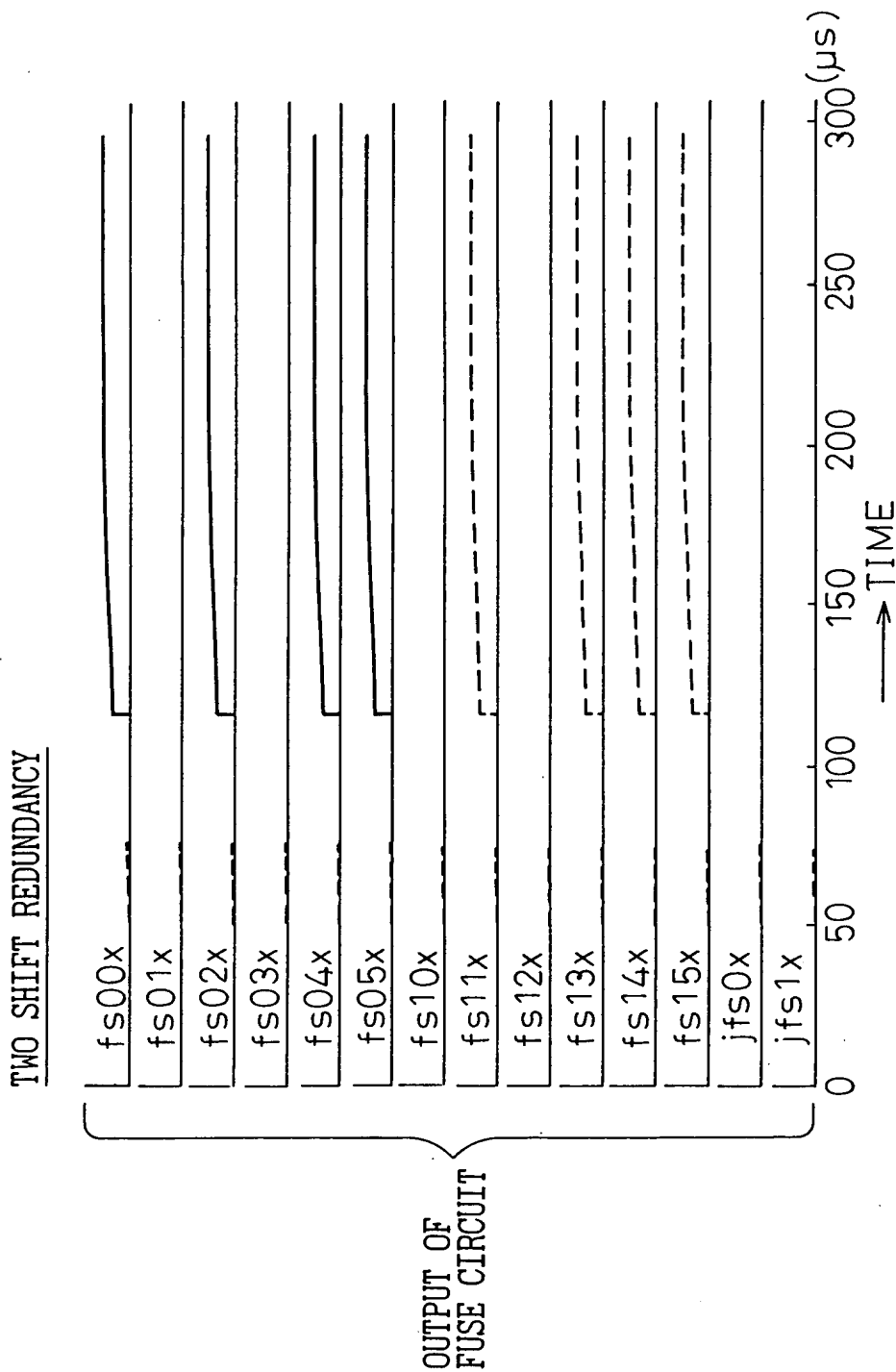
Fig. 48





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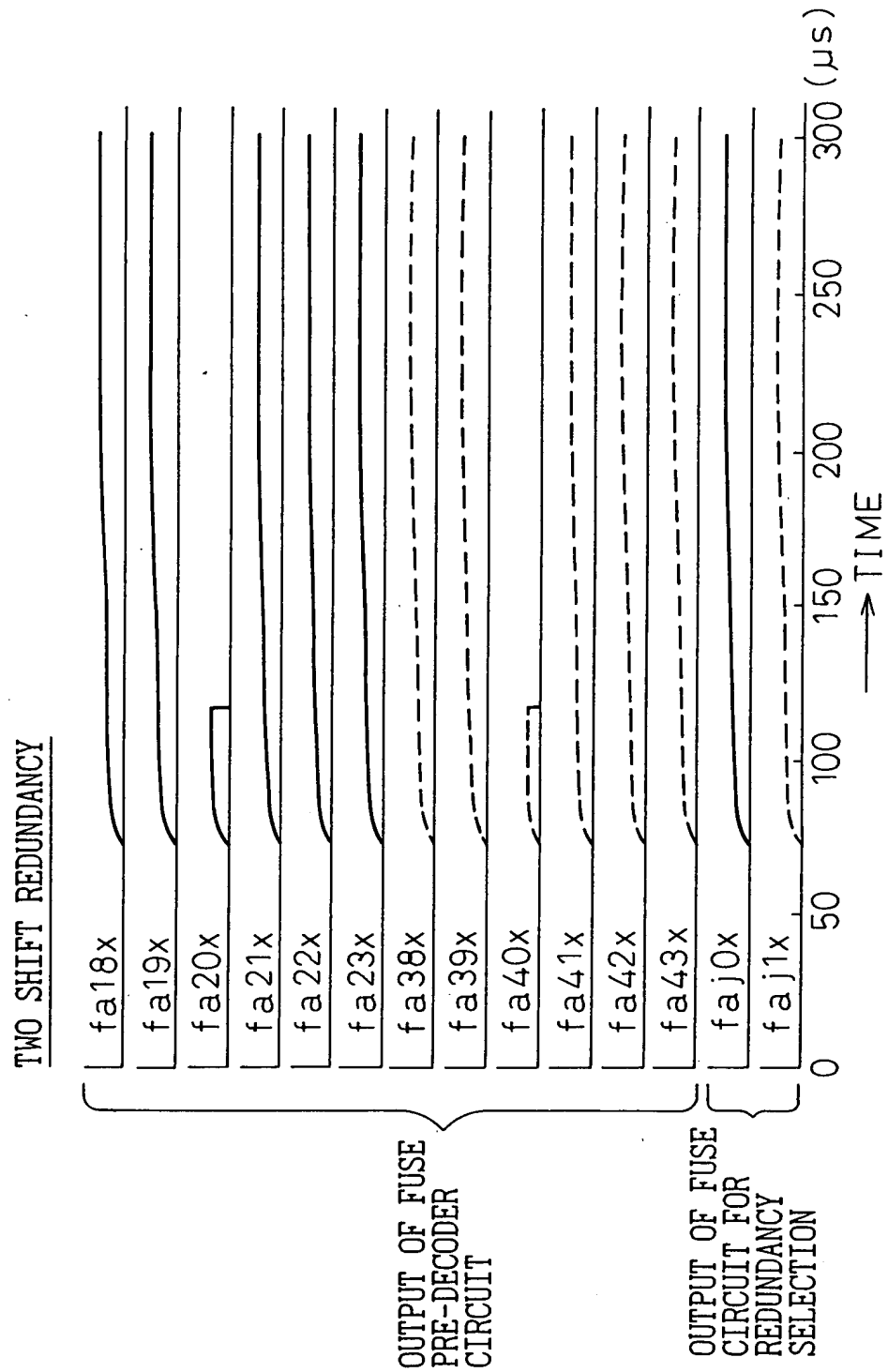
Fig. 49





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Fig. 50

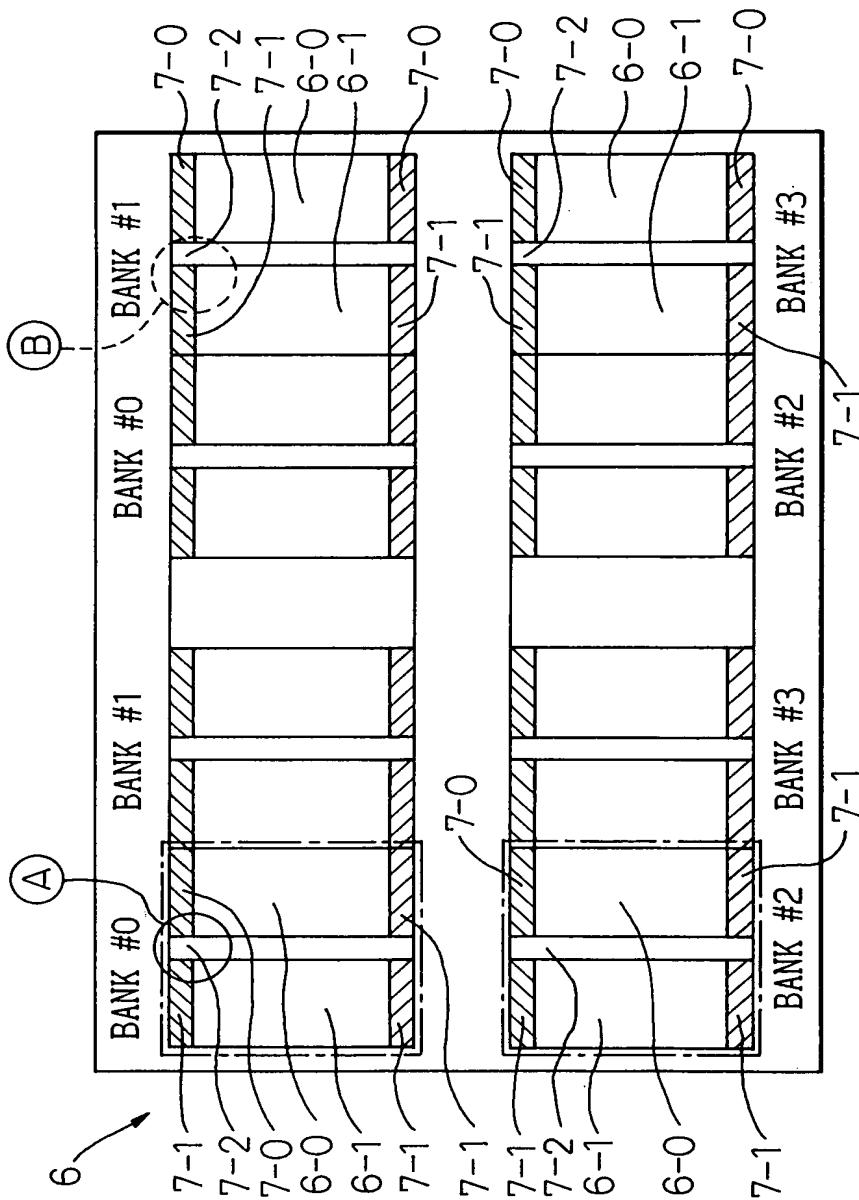




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Fig. 51

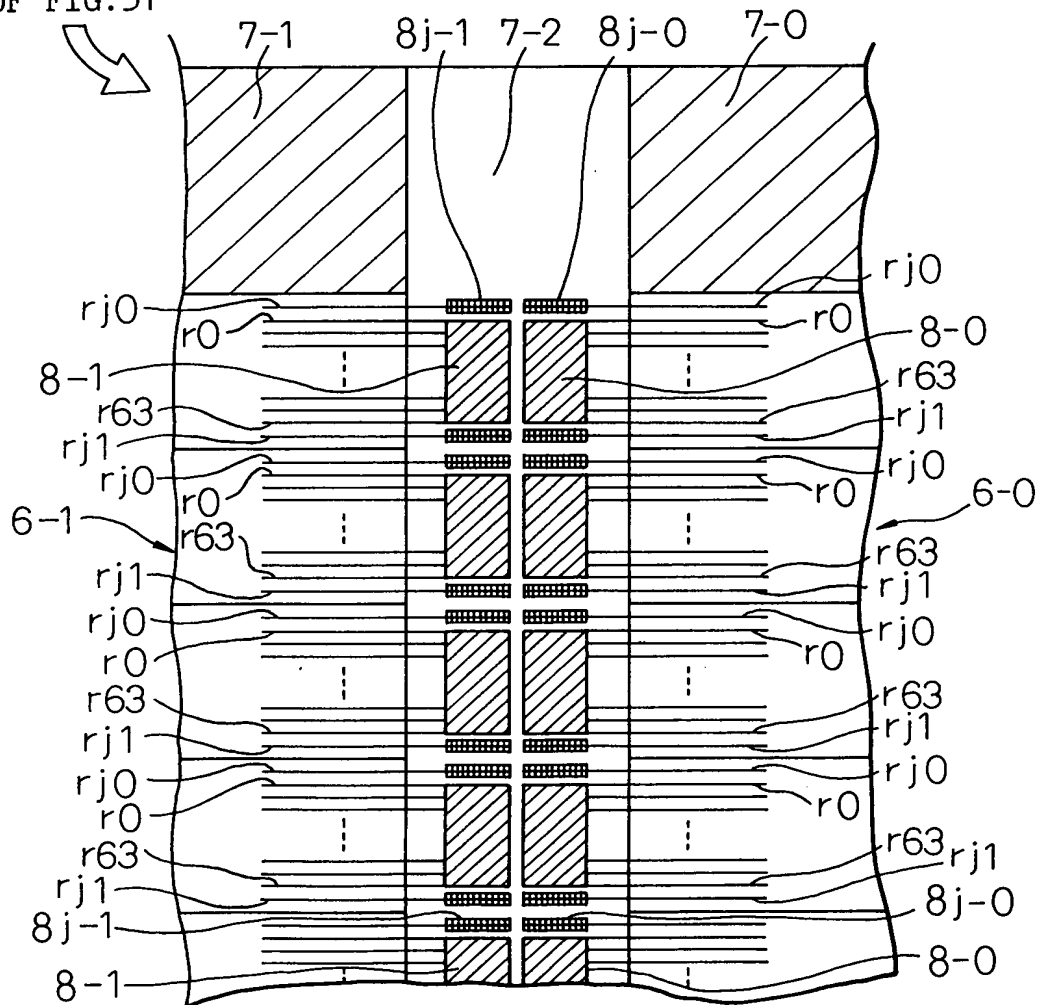




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Fig. 52

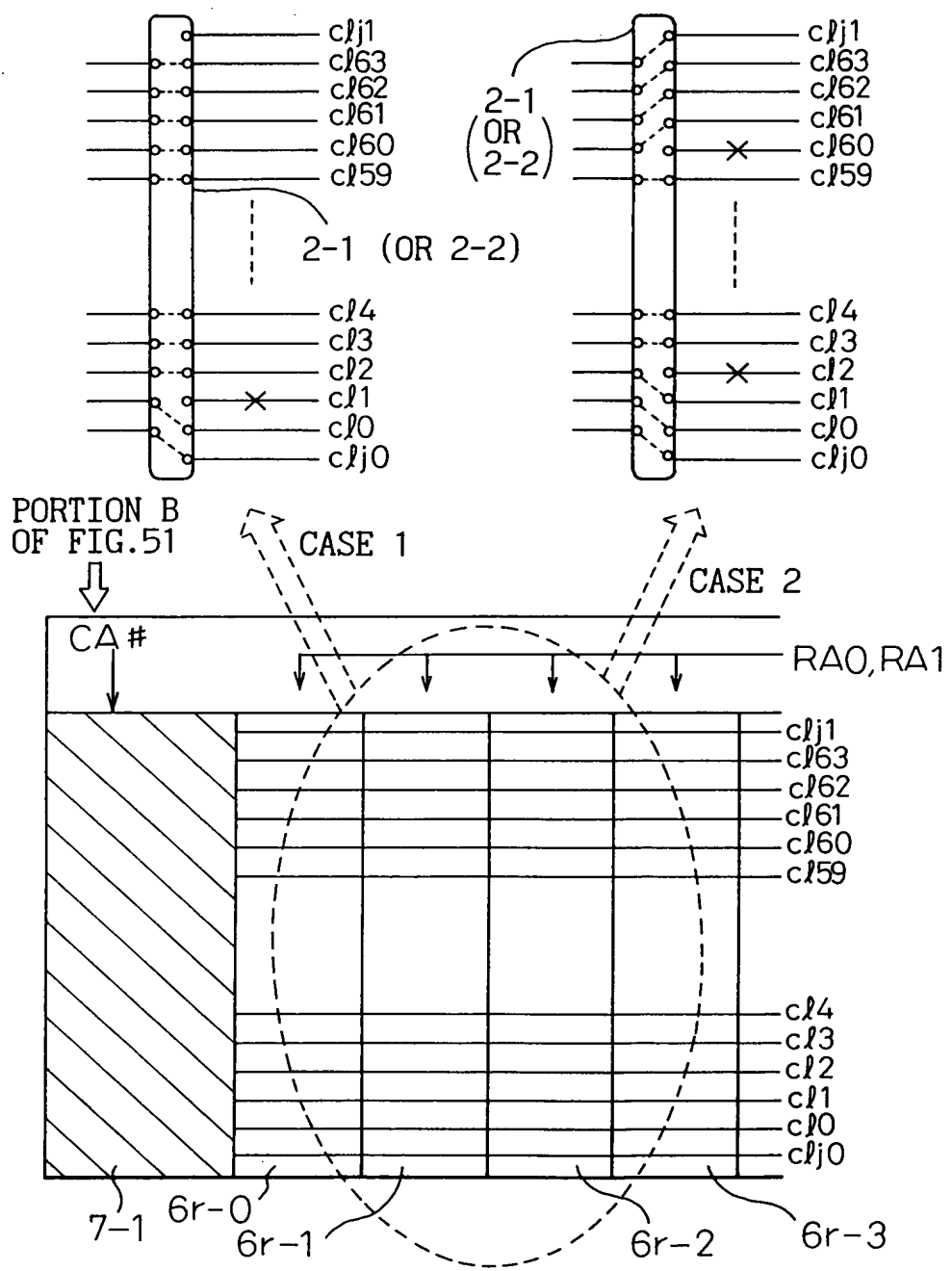
PORTION A
OF FIG. 51





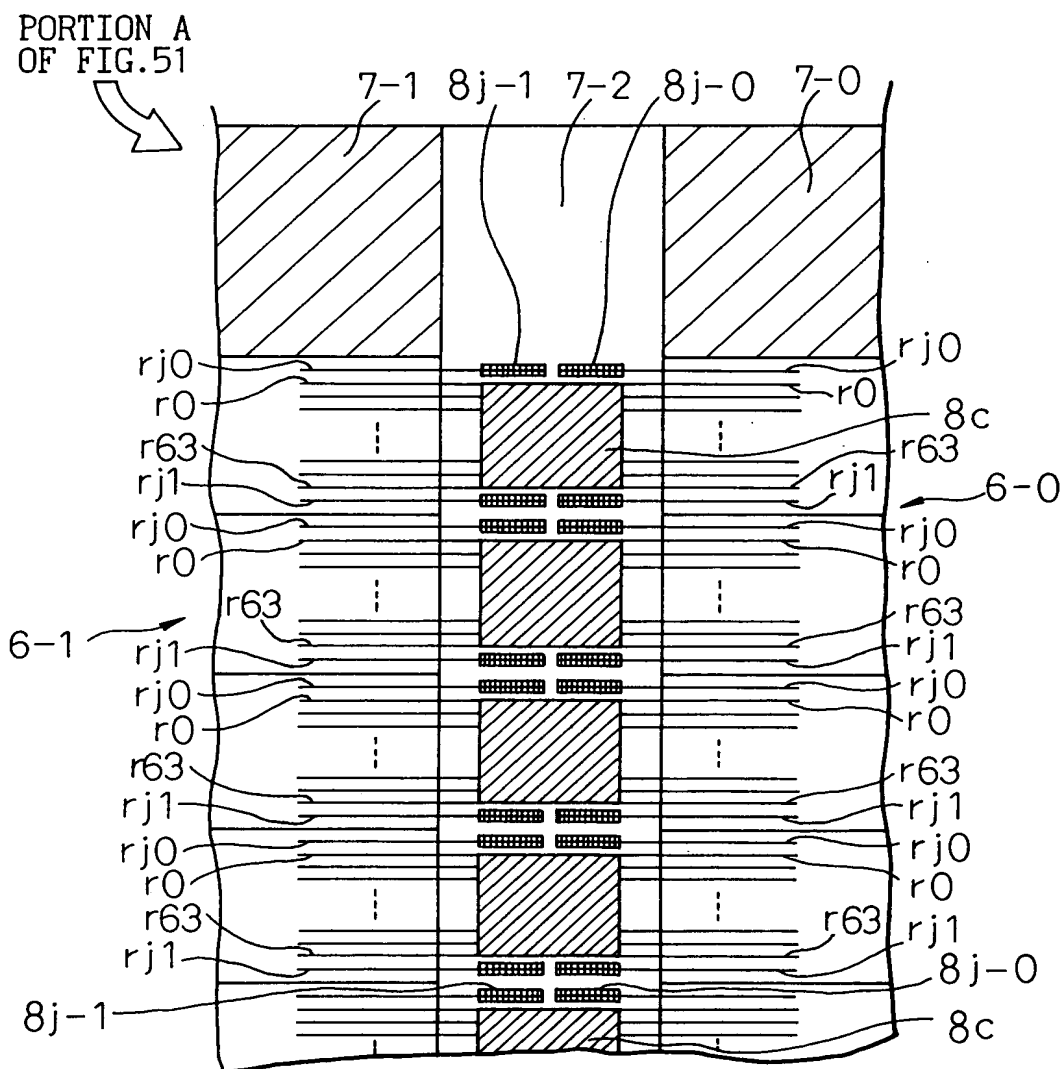
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Fig.53




$$\frac{48}{87}$$

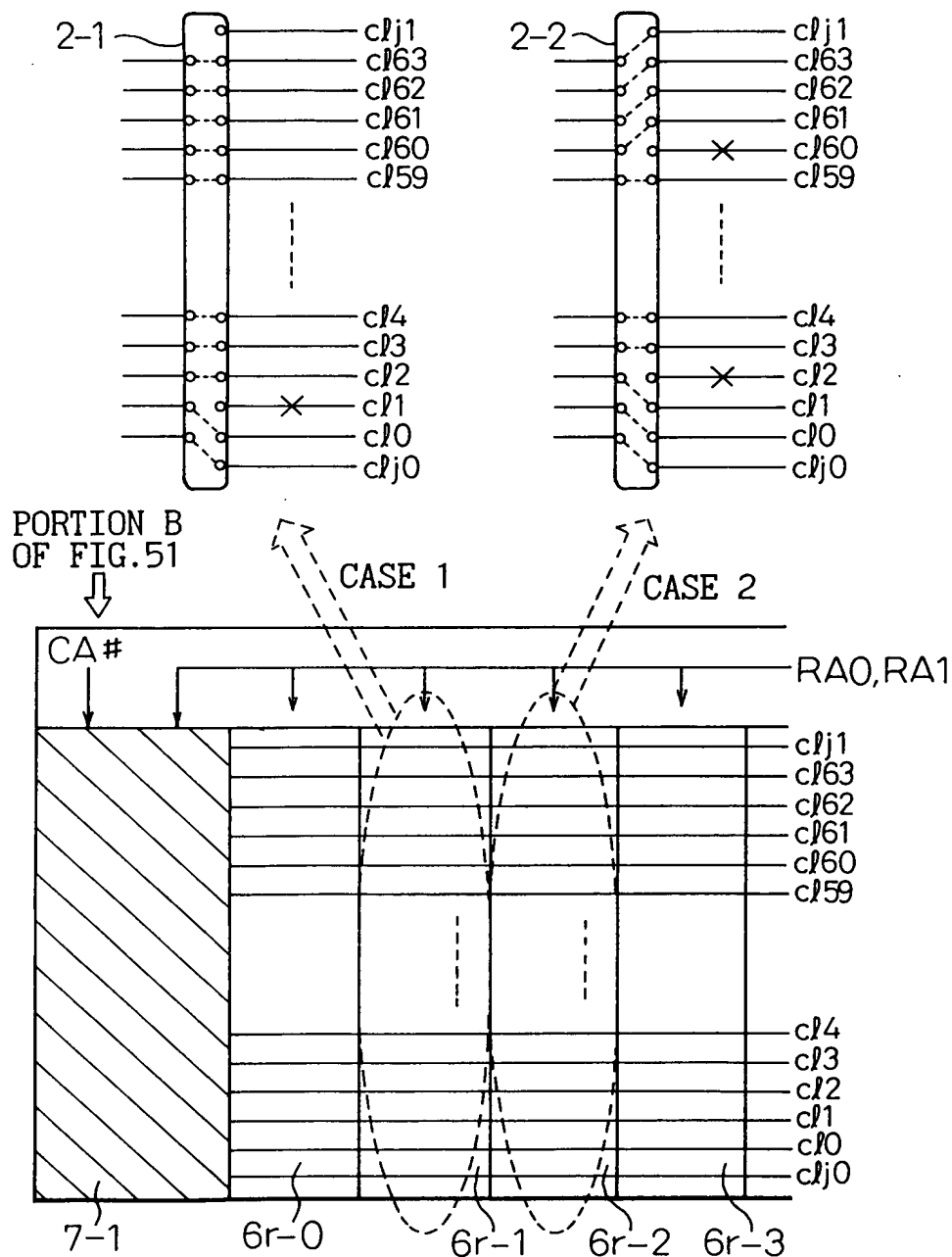
Fig. 54





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Fig. 55



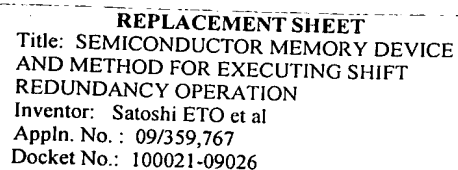

$$\frac{50}{87}$$

Fig. 56

SIDE OF CELL ARRAY No.1

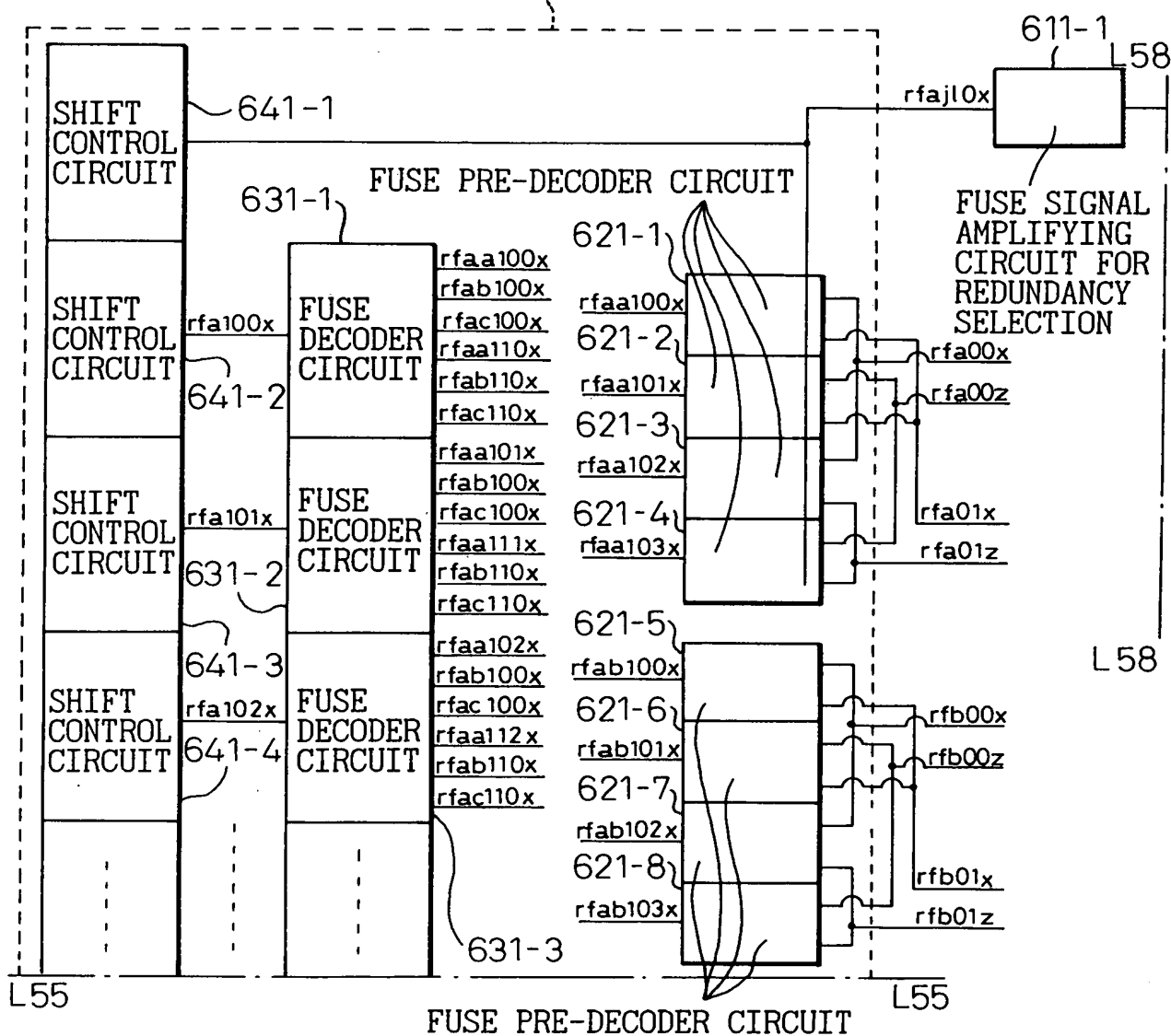
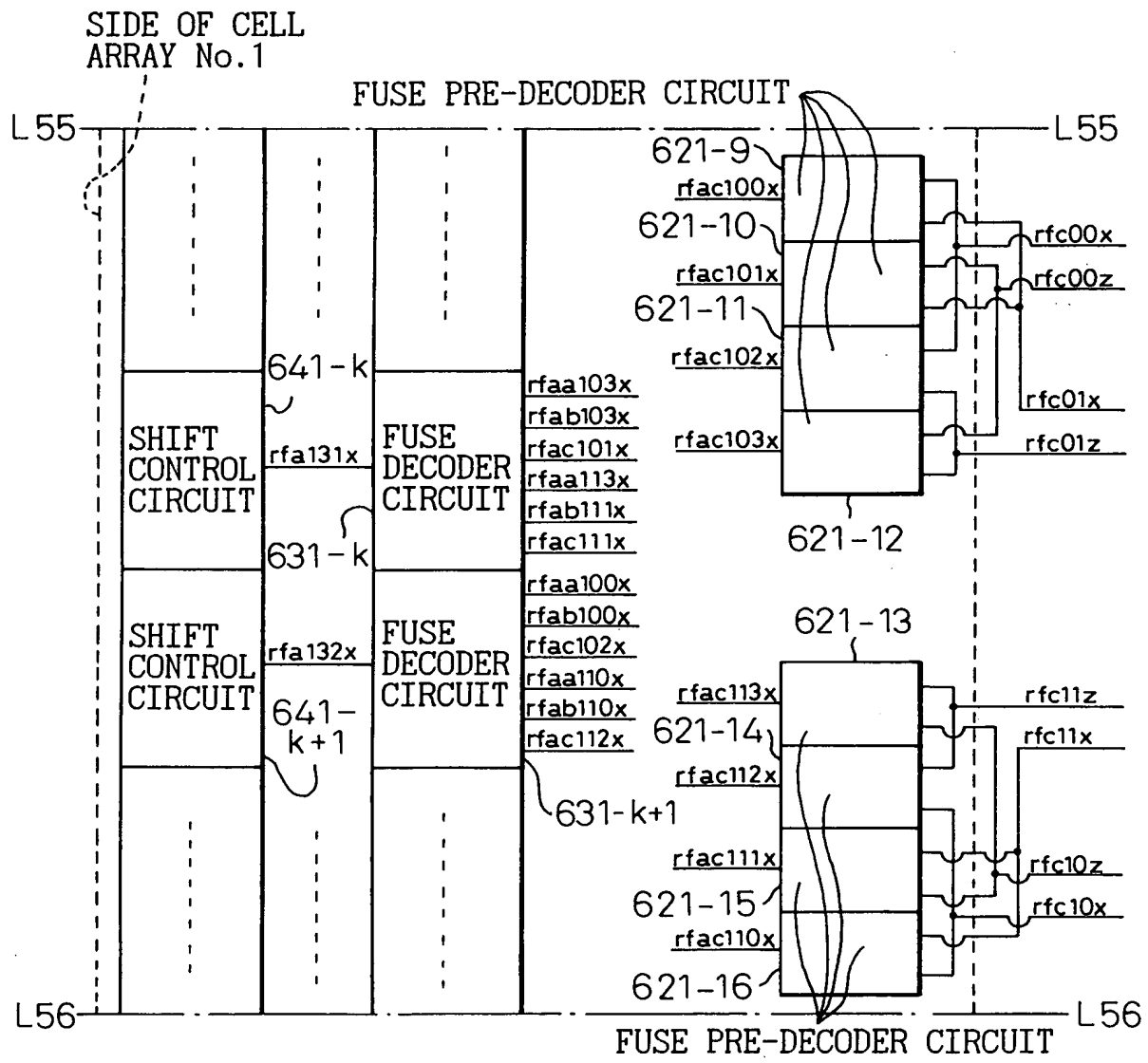
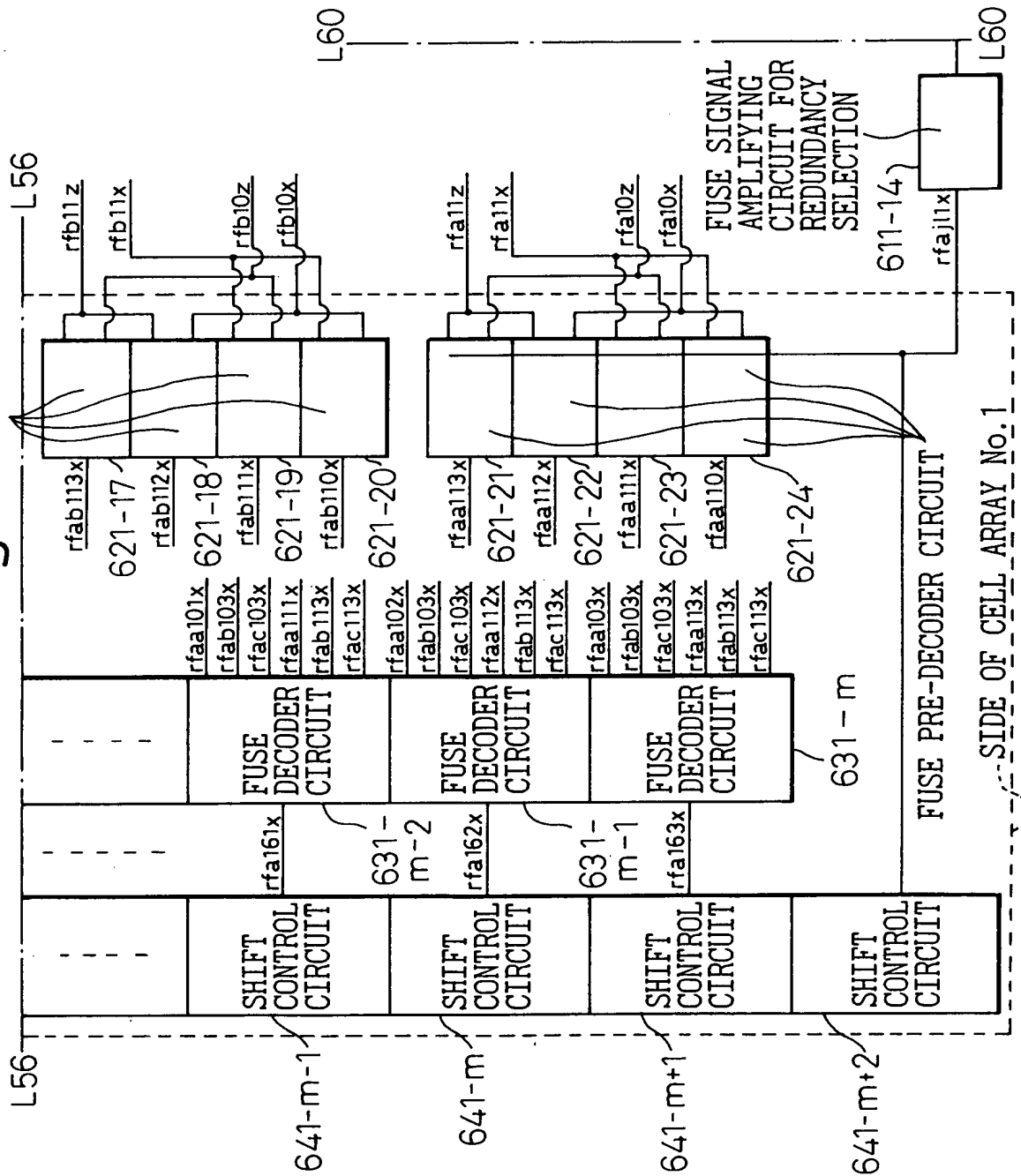
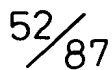
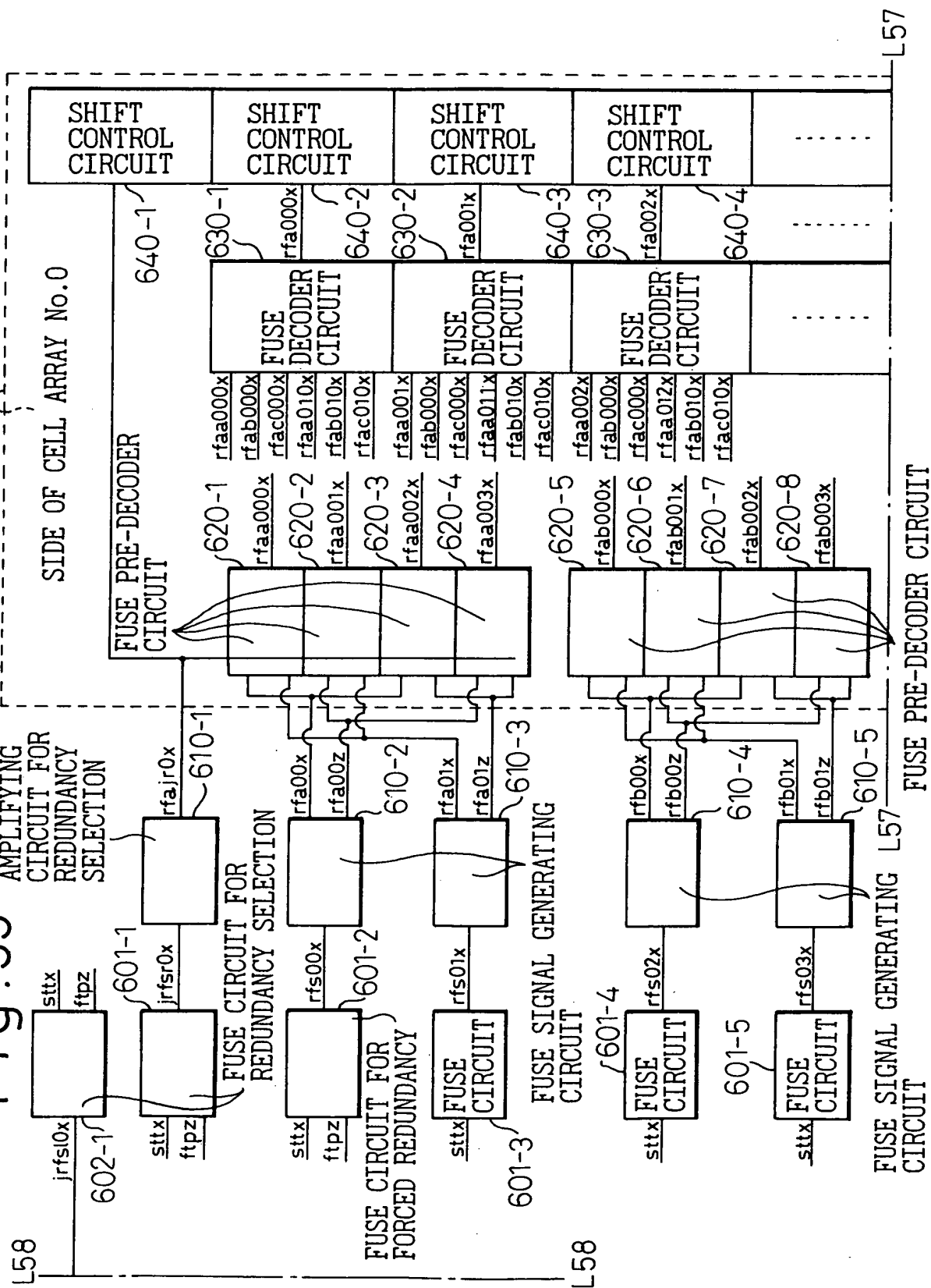
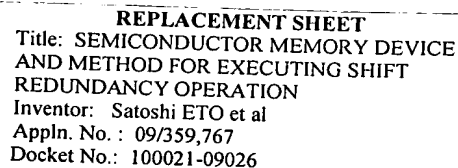




Fig.57



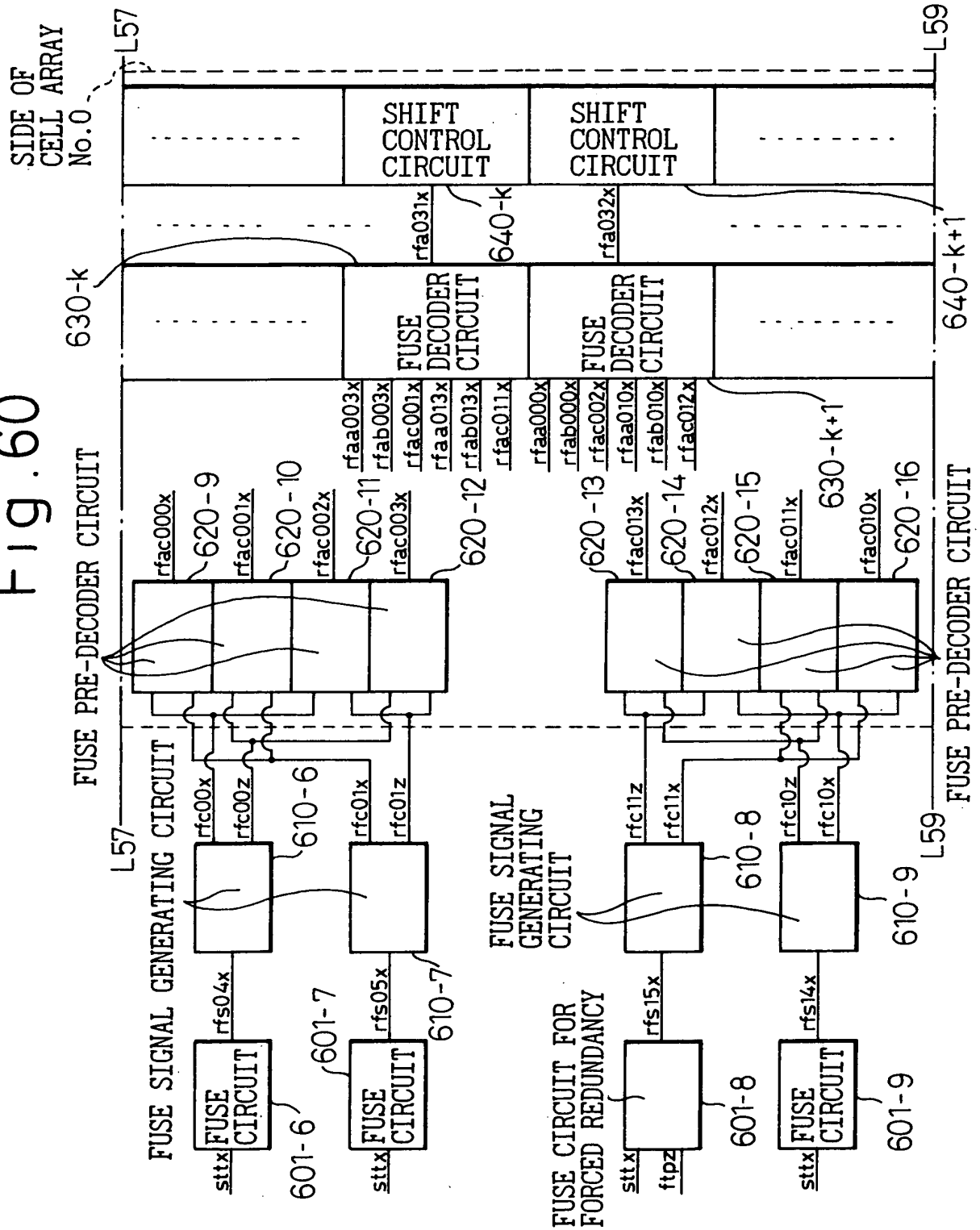






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Fig. 60



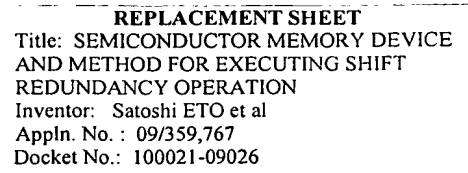


Fig. 61

The diagram illustrates a redundancy selection circuit, labeled Fig. 61. It is organized into three main functional blocks: FUSE SIGNAL GENERATING CIRCUIT, FUSE PRE-DECODER CIRCUIT, and FUSE SIGNAL AMPLIFYING CIRCUIT FOR REDUNDANCY SELECTION.

FUSE SIGNAL GENERATING CIRCUIT: This block contains two FUSE CIRCUIT blocks (601-11 and 601-12) and two FUSE CIRCUIT blocks (601-13 and 601-14). Each FUSE CIRCUIT block receives inputs from a set of FUSE SIGNALS (rfb11x, rfb12x, rfb13x, rfb14x) and outputs a FUSE SIGNAL (sttx, fttx, fttx, fttx).

FUSE PRE-DECODER CIRCUIT: This block contains two FUSE PRE-DECODER CIRCUIT blocks (620-17 and 620-24). Each FUSE PRE-DECODER CIRCUIT block receives inputs from a set of FUSE SIGNALS (rfab013x, rfab012x, rfab011x, rfab010x) and outputs a FUSE SIGNAL (rfaa001x, rfaa002x, rfaa003x, rfaa004x).

FUSE SIGNAL AMPLIFYING CIRCUIT FOR REDUNDANCY SELECTION: This block contains two FUSE SIGNAL AMPLIFYING CIRCUIT FOR REDUNDANCY SELECTION blocks (640-m and 640-m+1). Each FUSE SIGNAL AMPLIFYING CIRCUIT FOR REDUNDANCY SELECTION block receives inputs from a set of FUSE SIGNALS (rfab013x, rfab012x, rfab011x, rfab010x) and outputs a FUSE SIGNAL (rfaa001x, rfaa002x, rfaa003x, rfaa004x).

The diagram also shows a series of FUSE SIGNALS (rfb11x, rfb12x, rfb13x, rfb14x) and FUSE SIGNALS (sttx, fttx, fttx, fttx) connected to the FUSE CIRCUIT blocks. The FUSE SIGNALS (rfab013x, rfab012x, rfab011x, rfab010x) are connected to the FUSE PRE-DECODER CIRCUIT blocks. The FUSE SIGNALS (rfaa001x, rfaa002x, rfaa003x, rfaa004x) are connected to the FUSE SIGNAL AMPLIFYING CIRCUIT FOR REDUNDANCY SELECTION blocks.

The diagram is labeled with "L59" at the top and "L60" at the bottom.



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Fig. 62

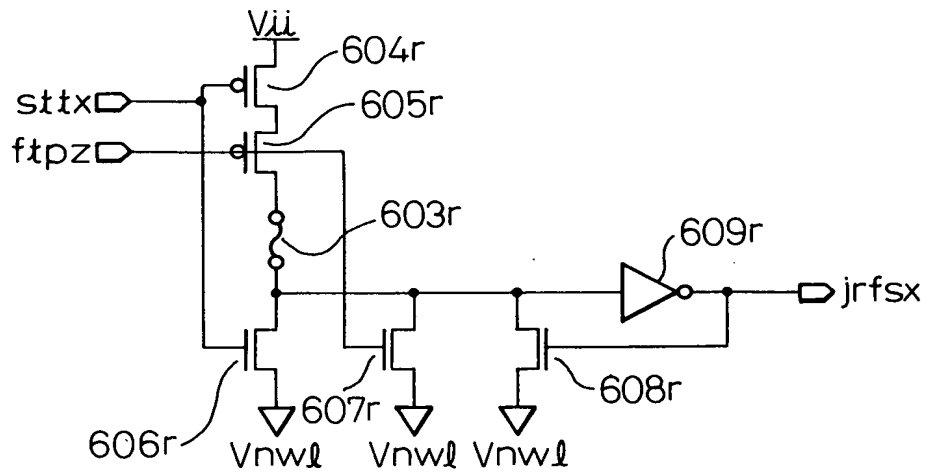
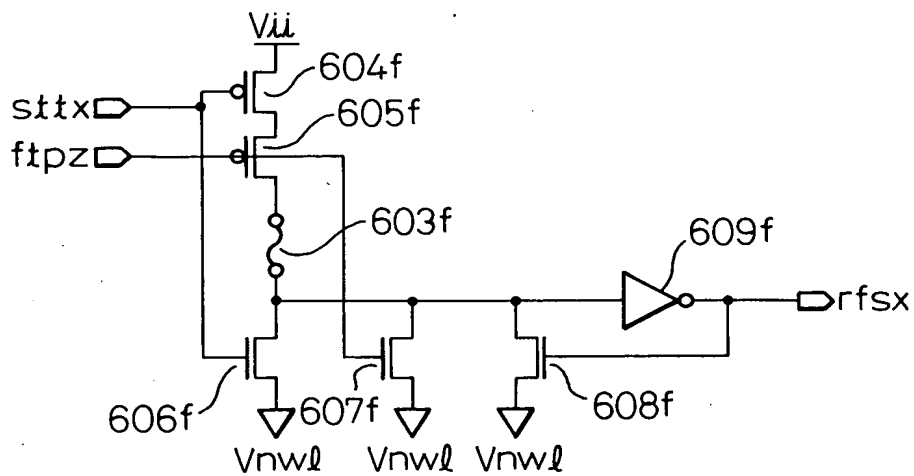


Fig. 63



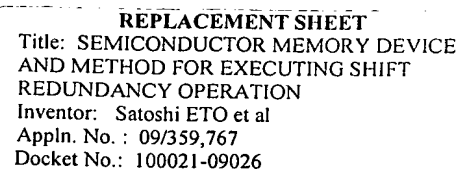
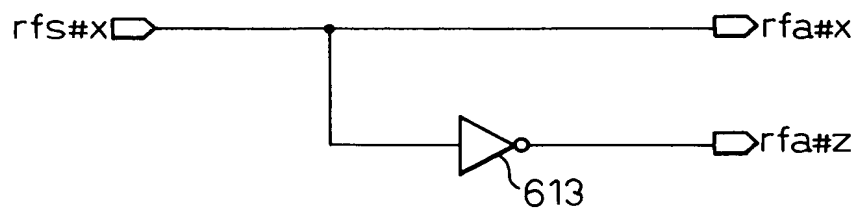


Fig. 64





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Fig. 67

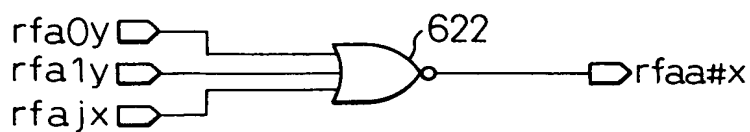


Fig. 68

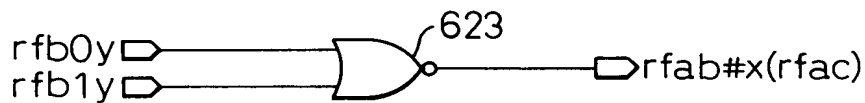
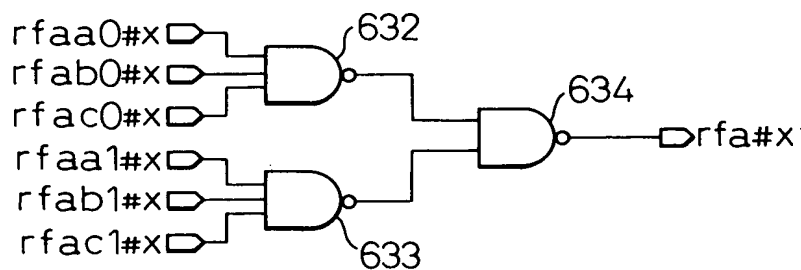


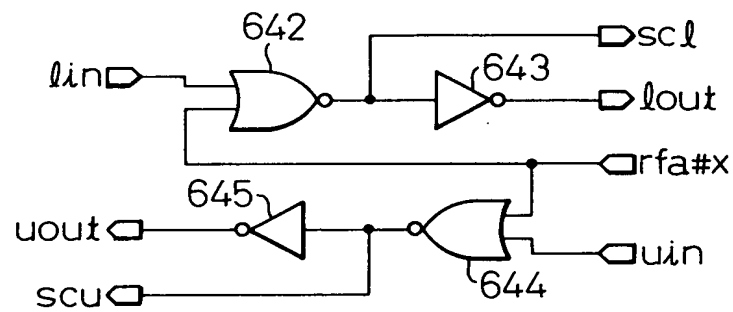
Fig. 69





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Fig.70



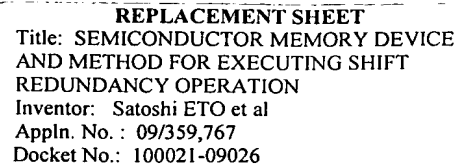
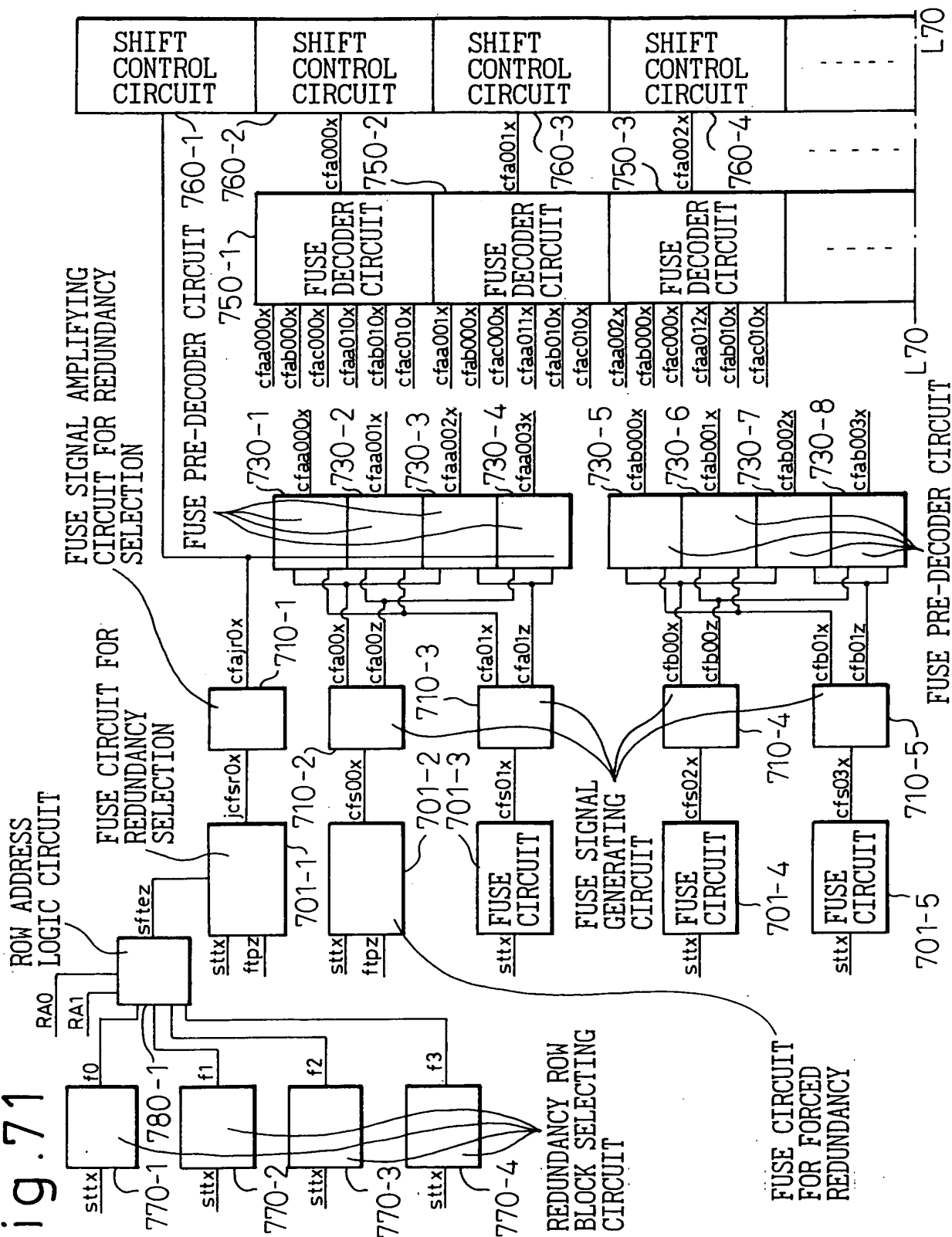

$$\frac{60}{87}$$

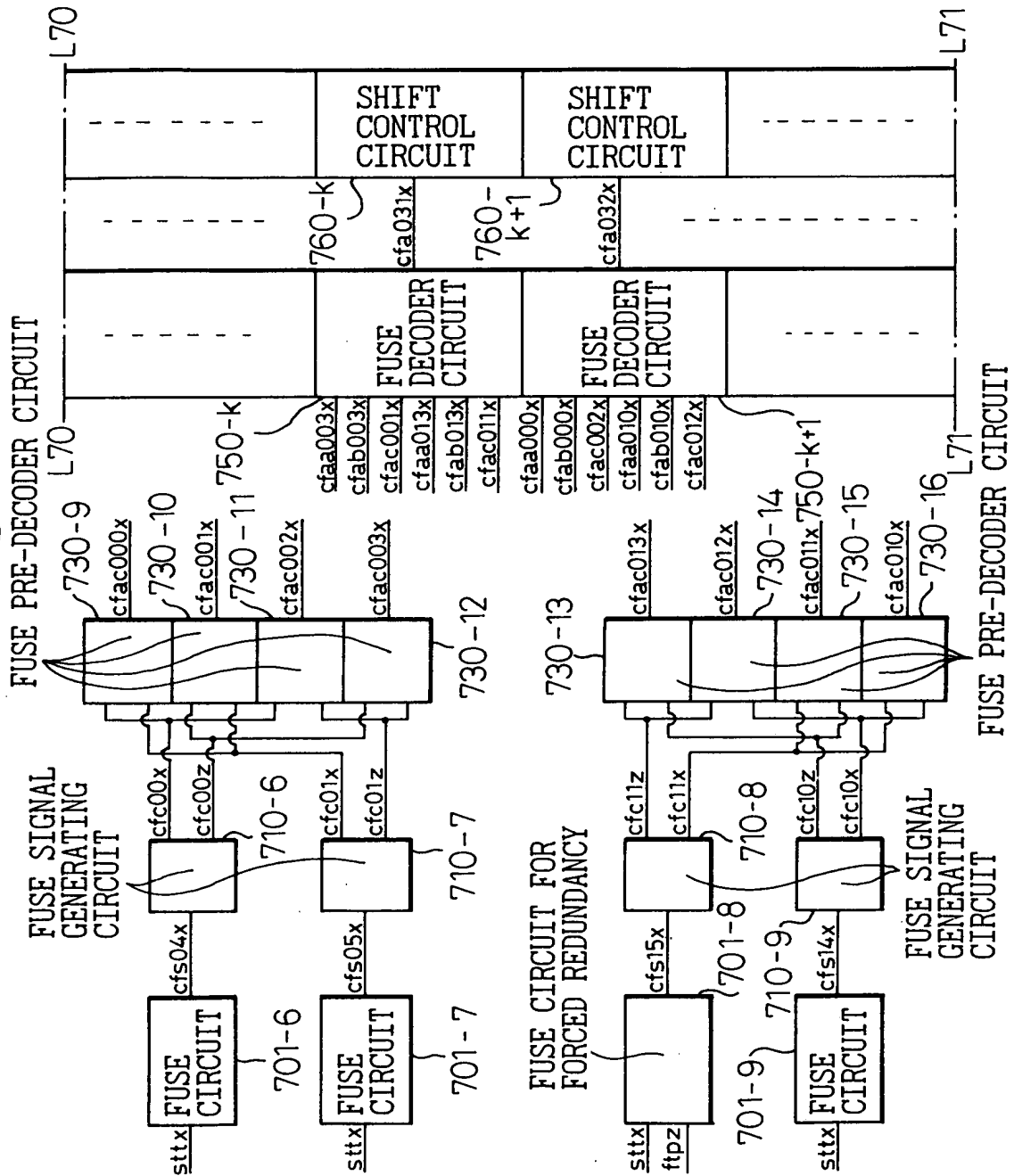
Fig. 71





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Fig. 72



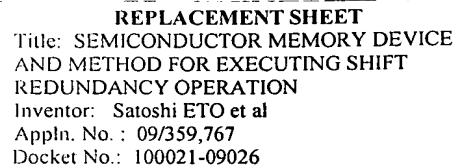
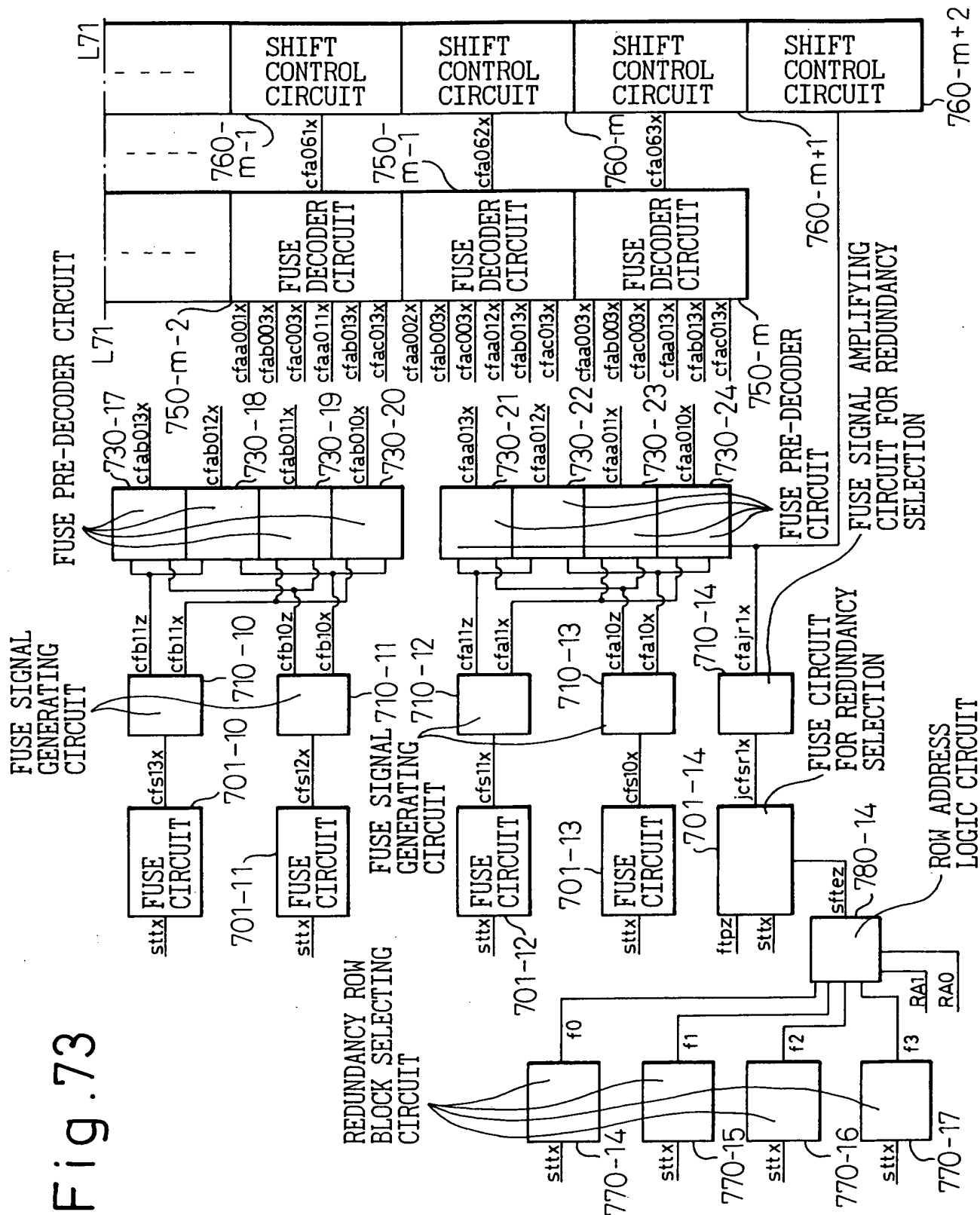

$$\frac{62}{87}$$

Fig. 73





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Fig.74

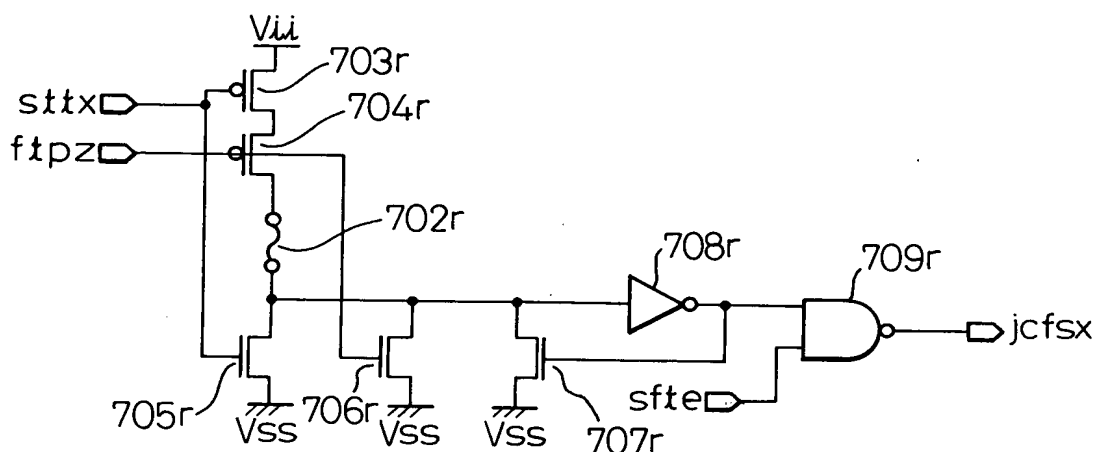
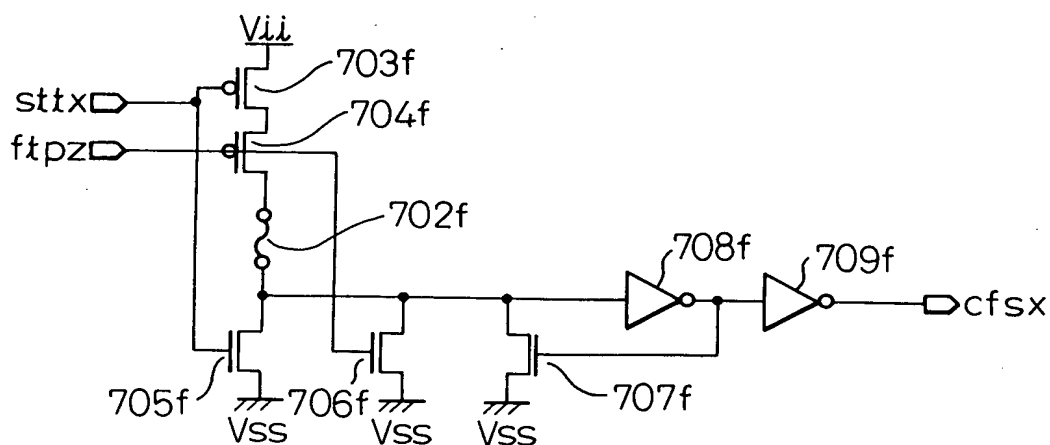


Fig.75





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Fig.76

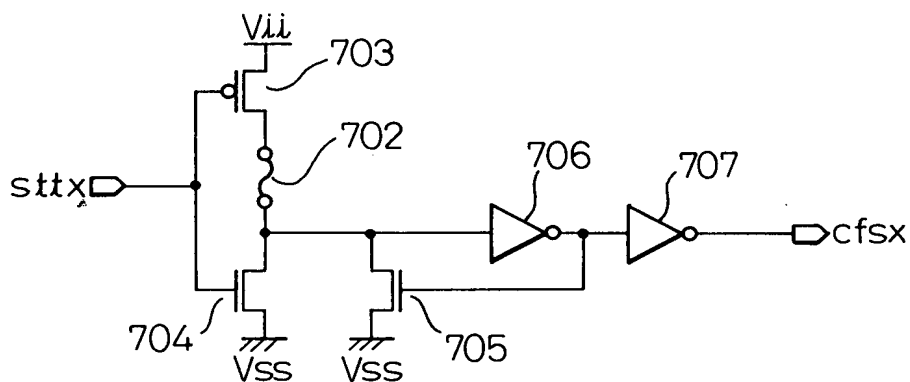
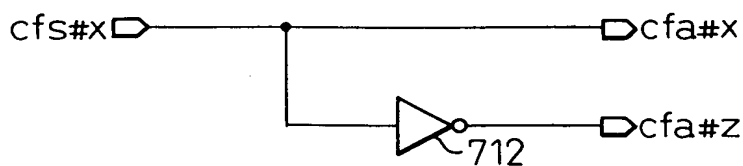


Fig.77



Fig.78





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Fig.79

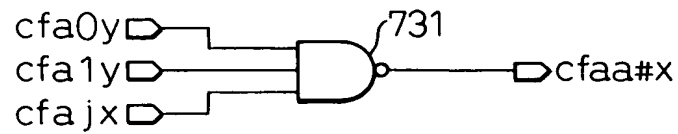


Fig.80

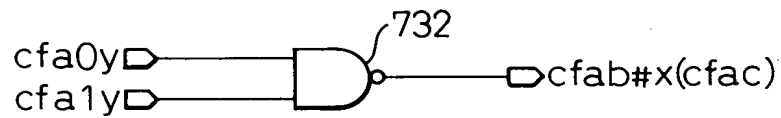
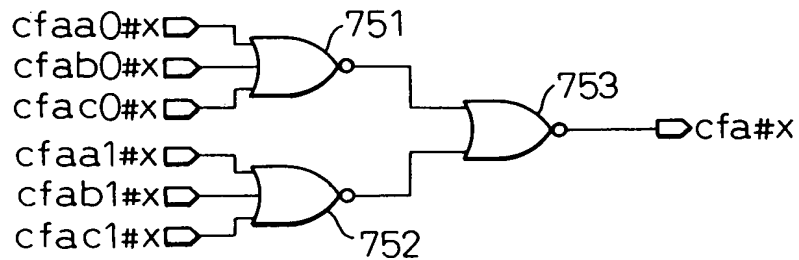


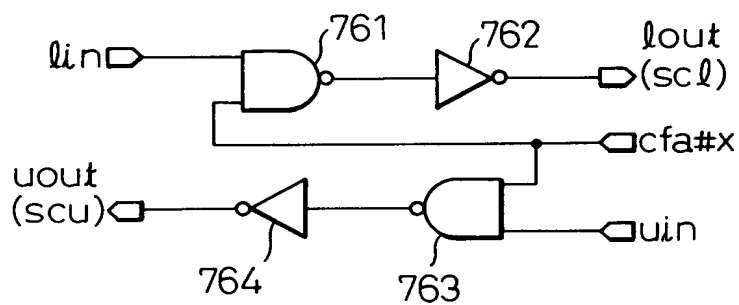
Fig.81





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Fig. 82

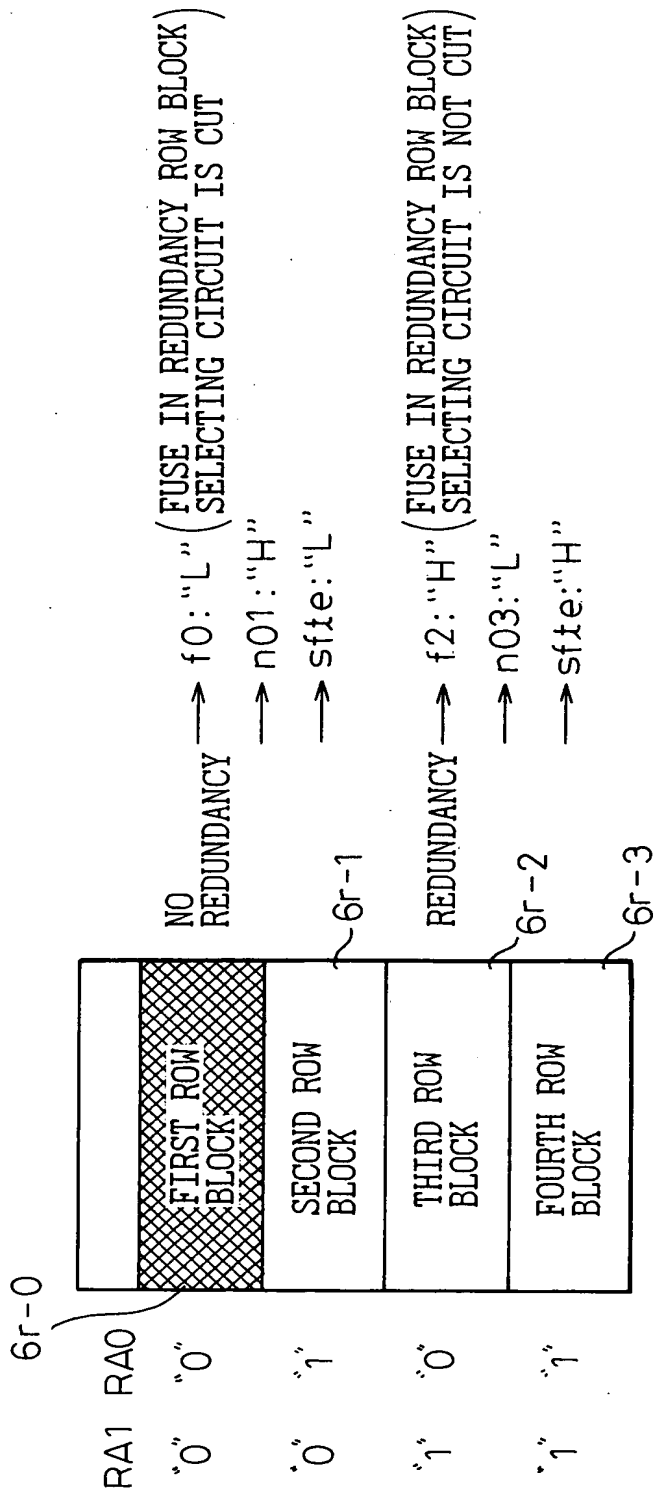




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REPLACEMENT SHEET
Title: SEMICONDUCTOR MEMORY DEVICE
AND METHOD FOR EXECUTING SHIFT
REDUNDANCY OPERATION
Inventor: Satoshi ETO et al
Appln. No.: 09/359,767
Docket No.: 100021-09026

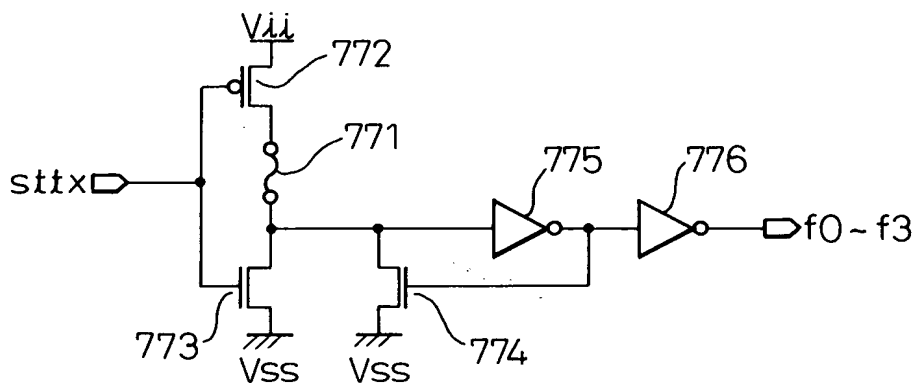
Fig. 83





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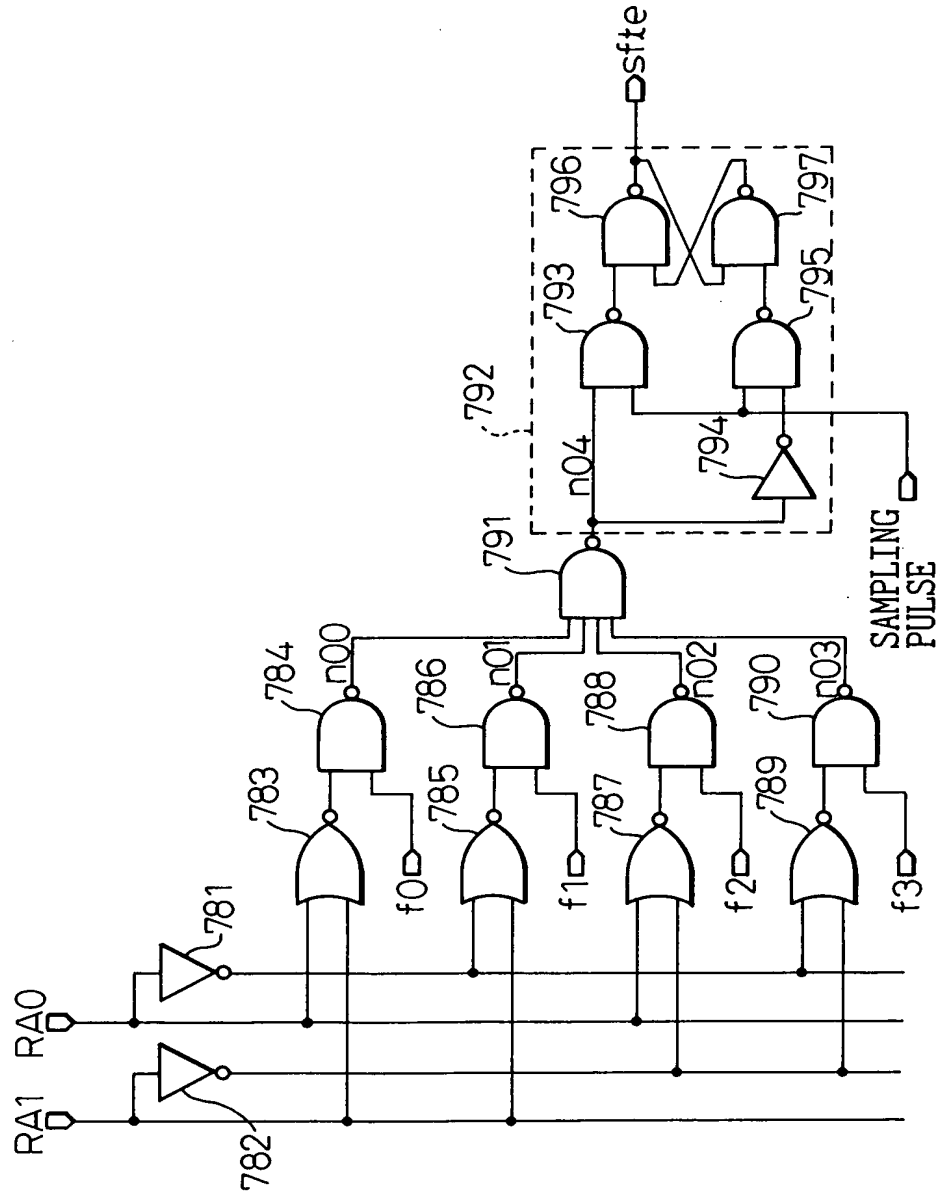
Fig.84





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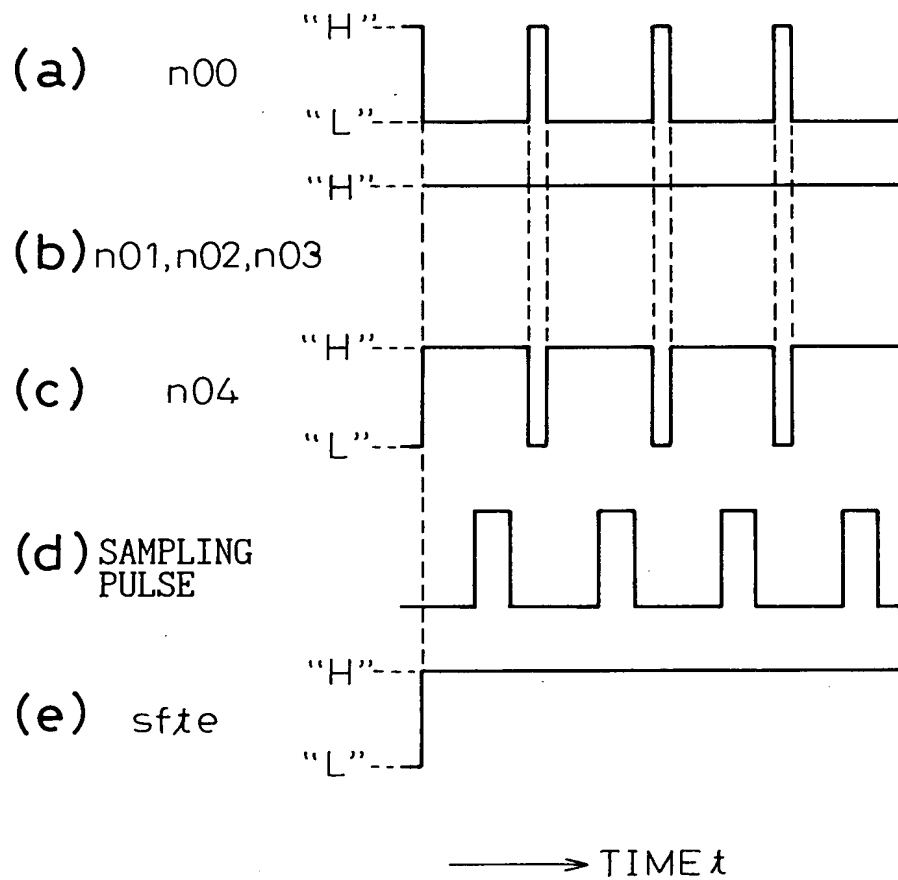
Fig. 85





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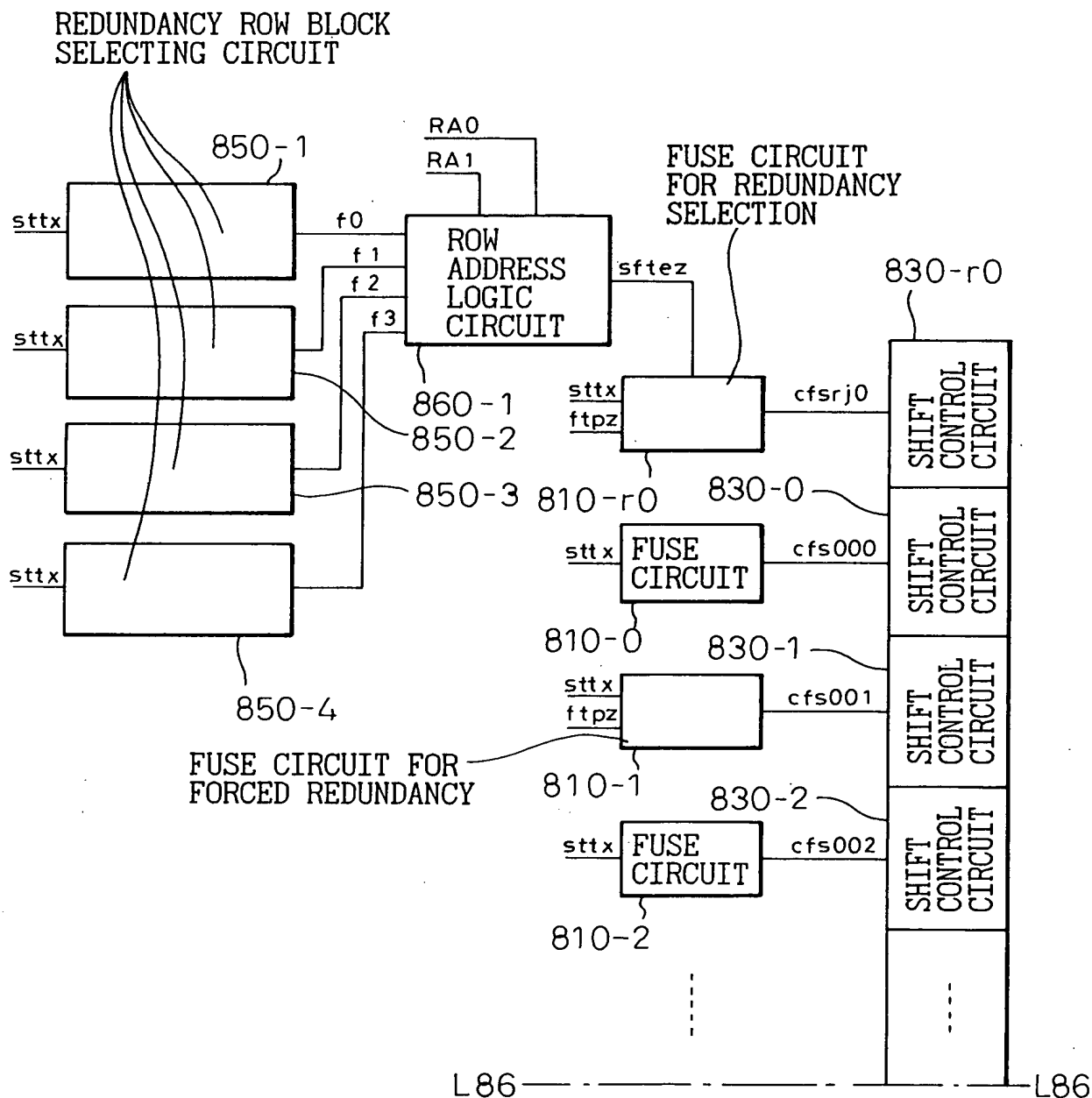
Fig. 86





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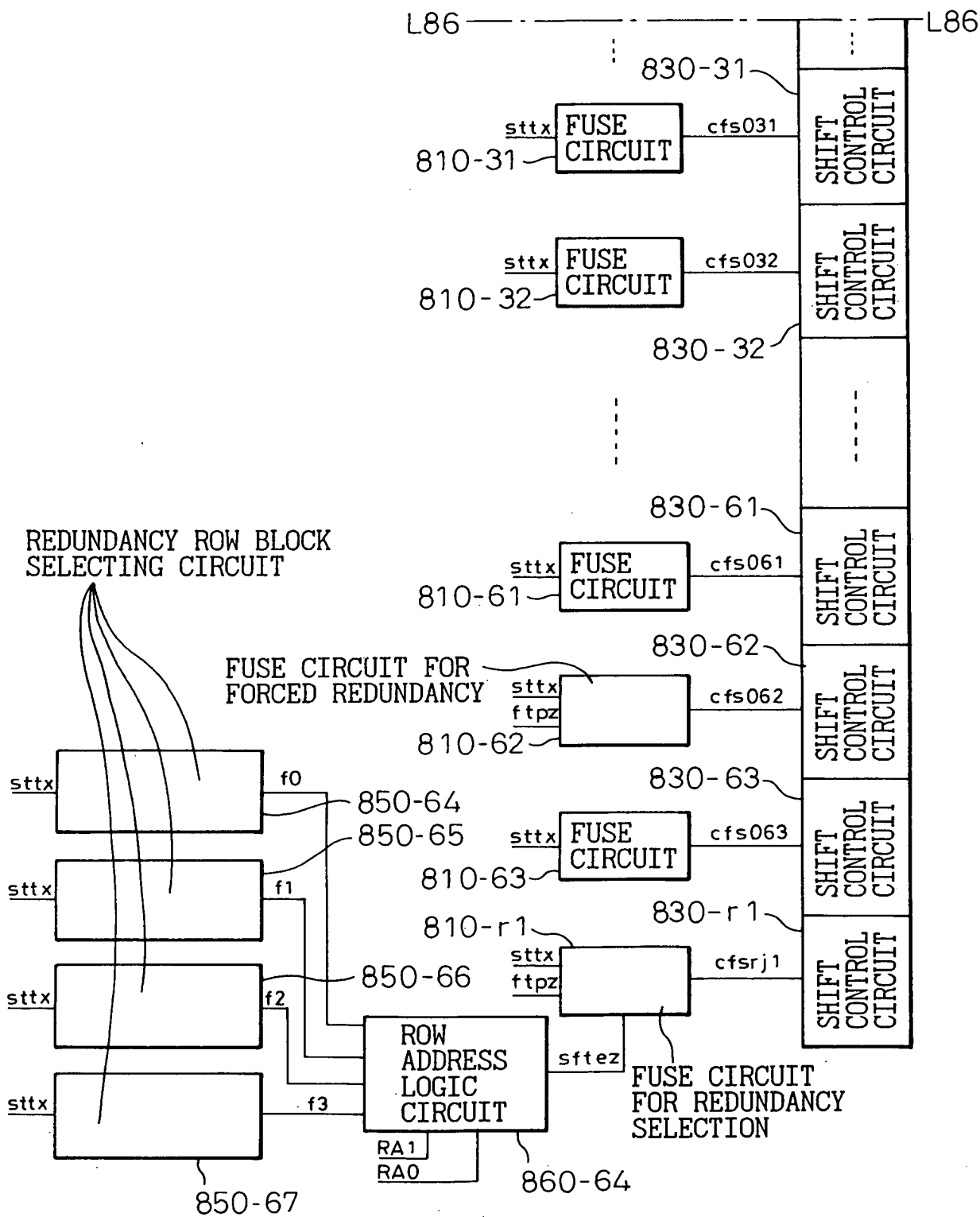
Fig.87





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Fig. 88





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Fig.89

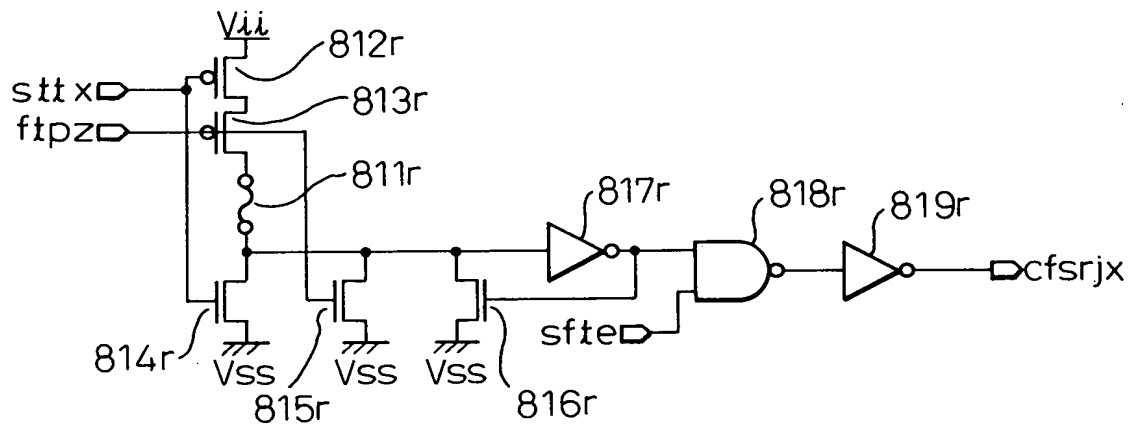
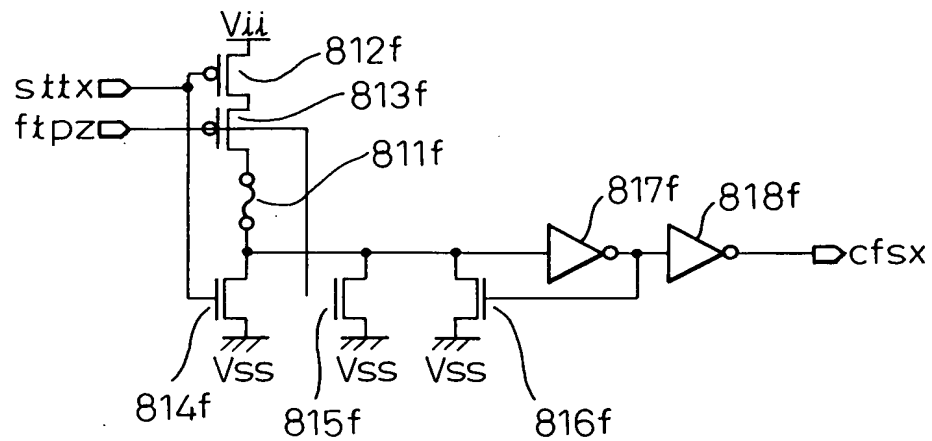


Fig.90





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REPLACEMENT SHEET
Title: SEMICONDUCTOR MEMORY DEVICE
AND METHOD FOR EXECUTING SHIFT
REDUNDANCY OPERATION
Inventor: Satōshi ETO et al
Appln. No.: 09/359,767
Docket No.: 100021-09026

Fig.91

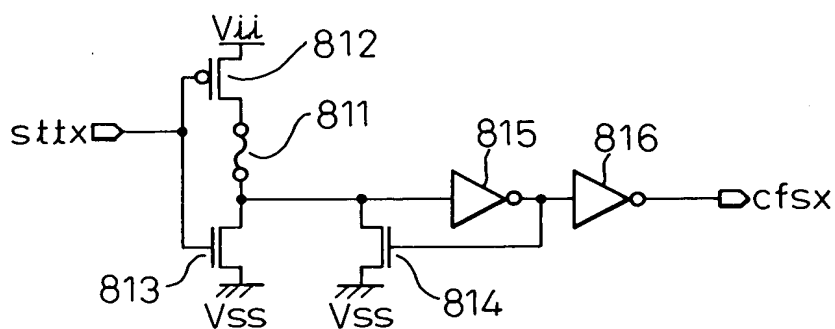
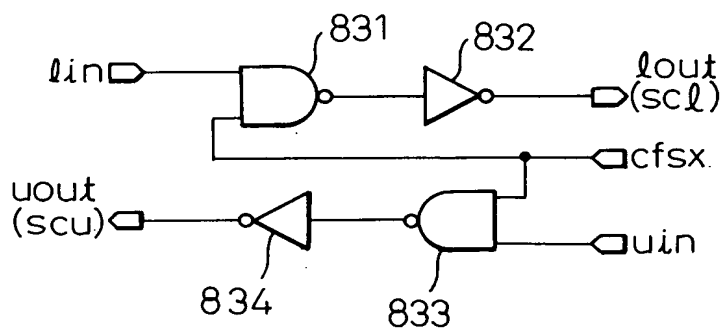


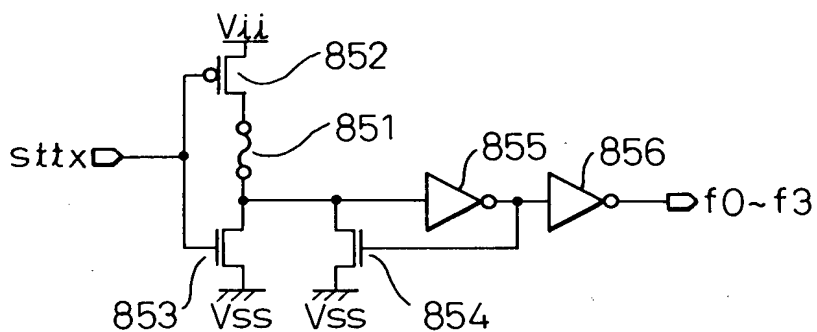
Fig.92





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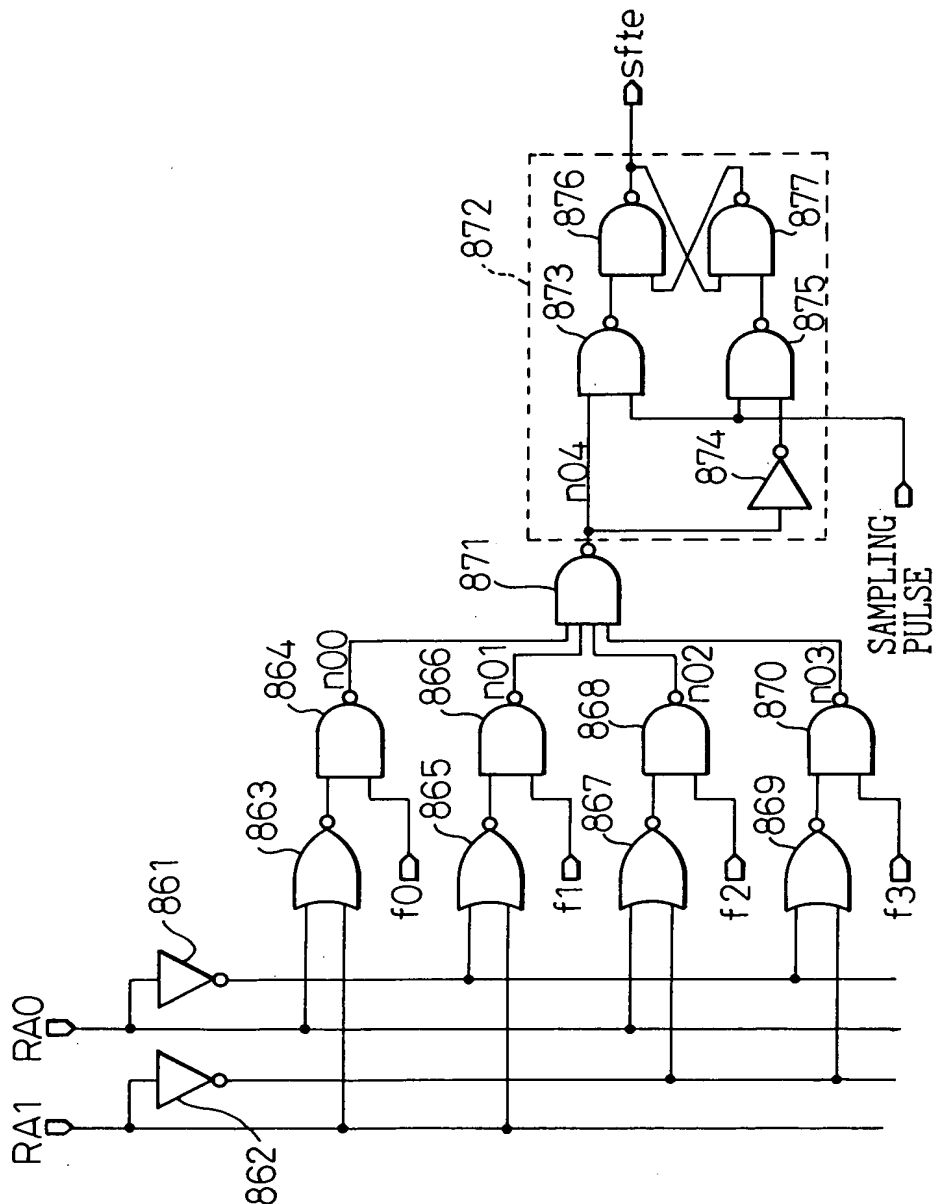
Fig. 93





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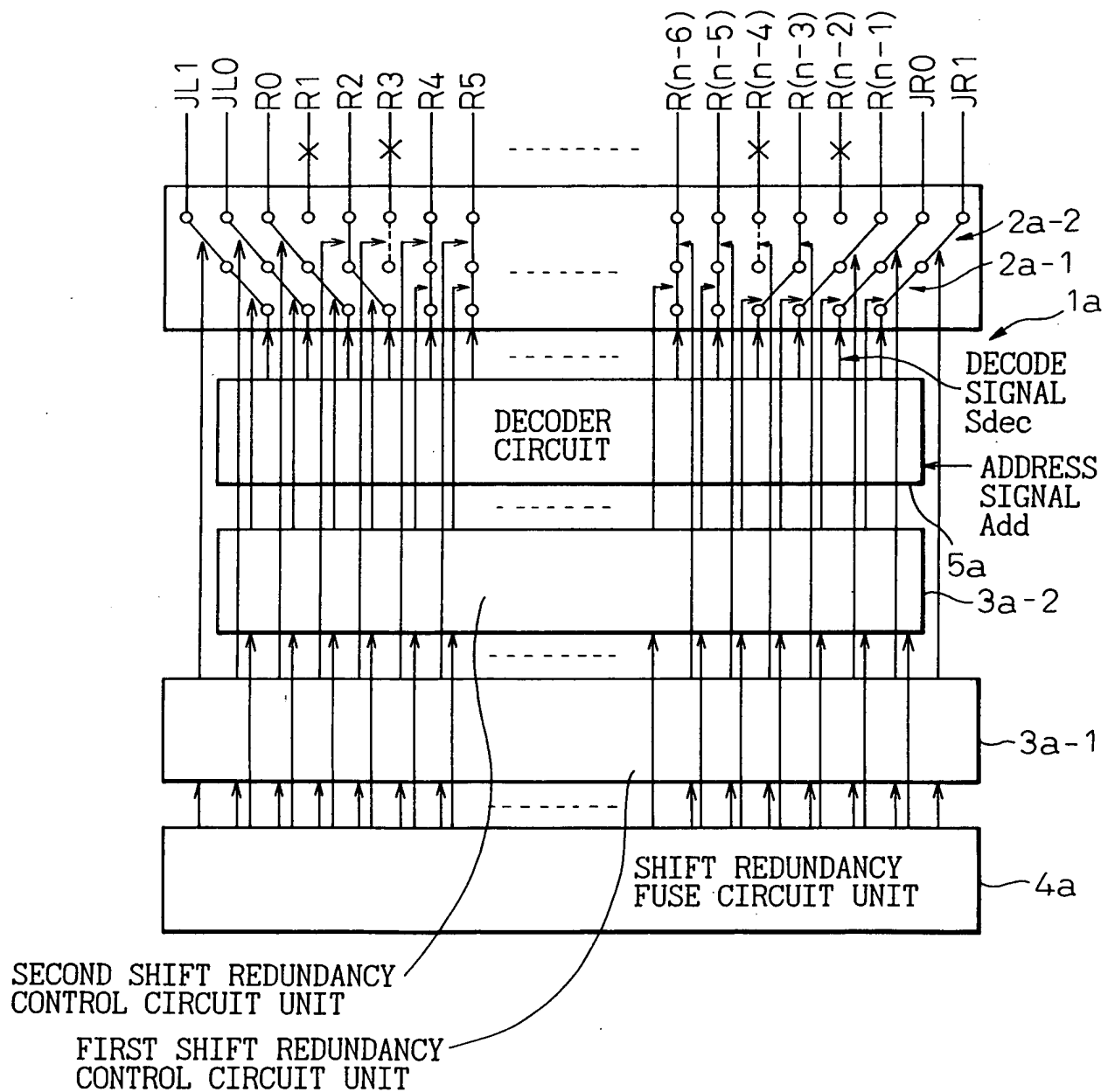
Fig. 94





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Fig. 95





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Fig.96

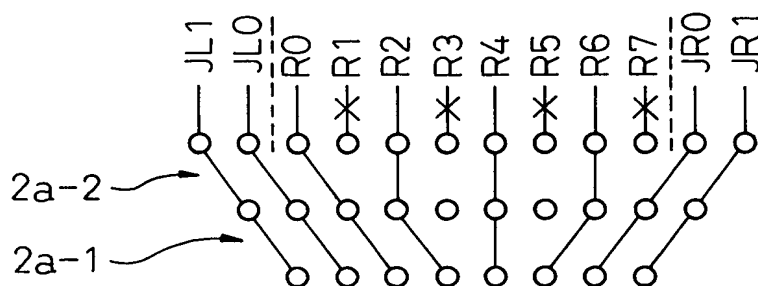


Fig.97

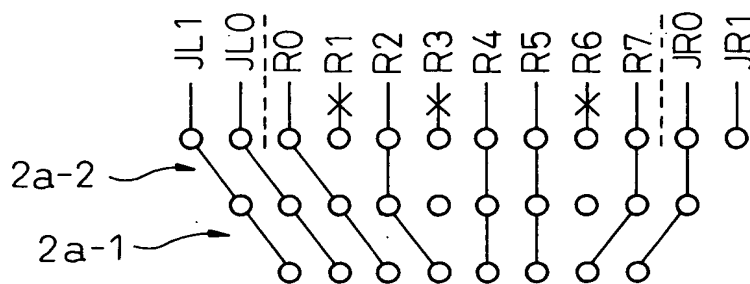
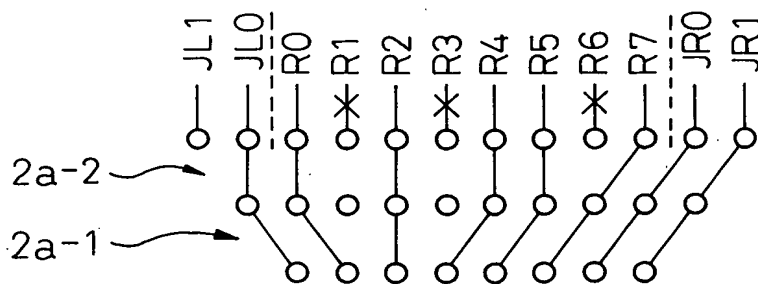


Fig.98





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Fig.99

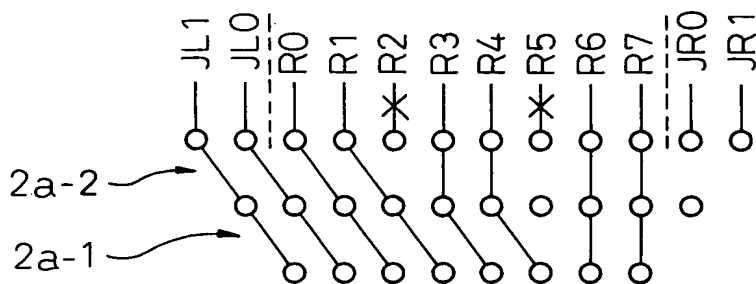


Fig.100

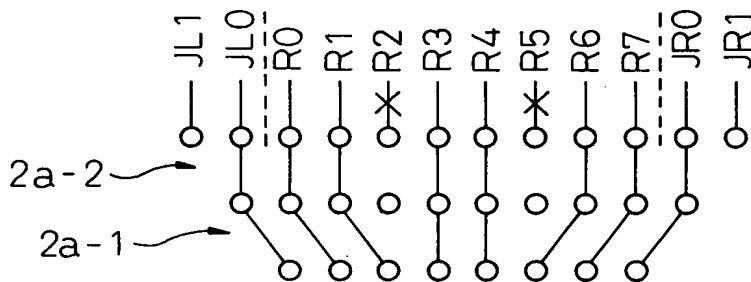
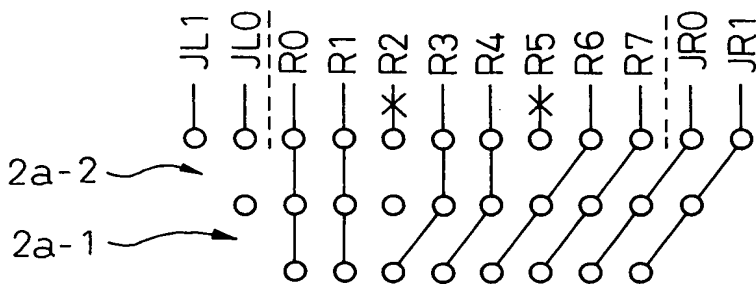


Fig.101





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Fig.102

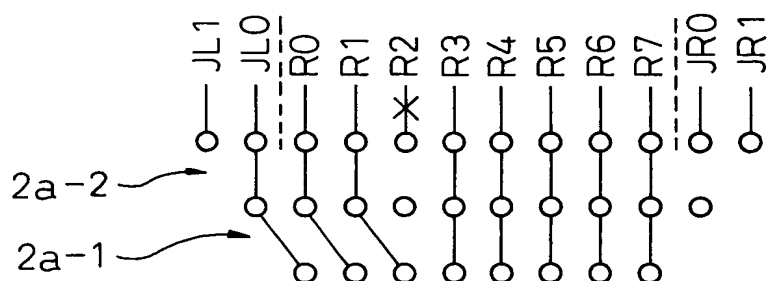


Fig.103

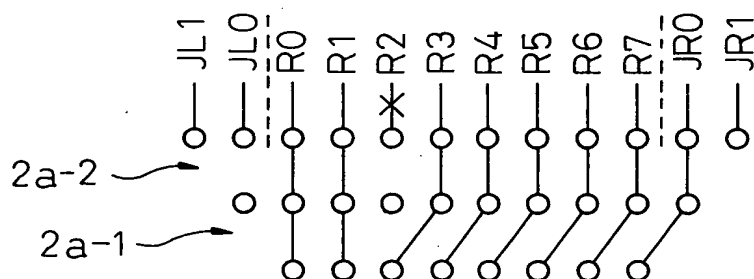
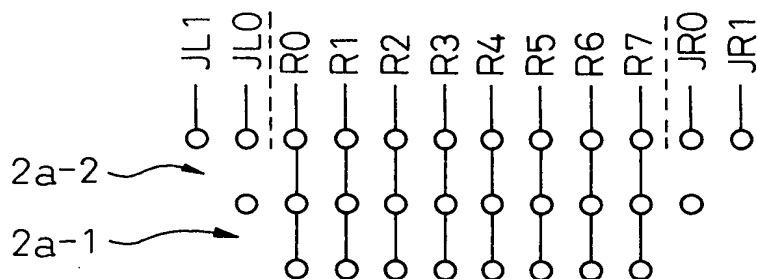


Fig.104





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Fig.105

SELECTING LINES	JL1	JL0	R0	R1	R2	R3	R4	R5	R6	R7	JR0	JR1
OUTPUT OF SECOND SHIFT REDUNDANCY CONTROL CIRCUIT UNIT	H L ←	H L ←	H L ←	L L X	L L ↑	L L X	L L ↑	L L X	L L ↑	L L X	L H ←	L H ←
OUTPUT OF FIRST SHIFT REDUNDANCY CONTROL CIRCUIT UNIT	H L ←	H L ←	H L ←	H L ←	H L ←	L L X	L L ↑	L L X	L L ↑	L L ↑	L H ←	L H ←
OUTPUT OF SHIFT REDUNDANCY FUSE CIRCUIT UNIT FUSE	H CUT	H CUT	H CUT	L CUT	H CUT	L CUT	H CUT	L CUT	H CUT	L CUT	H CUT	H CUT



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Fig.106

SELECTING LINES	JL1	JL0	R0	R1	R2	R3	R4	R5	R6	R7	JR0	JR1
OUTPUT OF SECOND SHIFT REDUNDANCY CONTROL CIRCUIT UNIT	H L ←	H L ←	H L ←	L L X	L L ↑	L L X	L L ↑	L L ↑	L L X	L L ↑	L L ↑	L L ↑
OUTPUT OF FIRST SHIFT REDUNDANCY CONTROL CIRCUIT UNIT	H L ←	H L ←	H L ←	H L ←	H L ←	L L X	L L ↑	L L ↑	L L X	L L ↑	L H ↑	L H ↑
OUTPUT OF SHIFT REDUNDANCY FUSE CIRCUIT UNIT	H CUT	H CUT	H CUT	L CUT	H CUT	L CUT	H CUT	H CUT	L CUT	H CUT	H CUT	L CUT


$$\frac{83}{87}$$

Fig.107

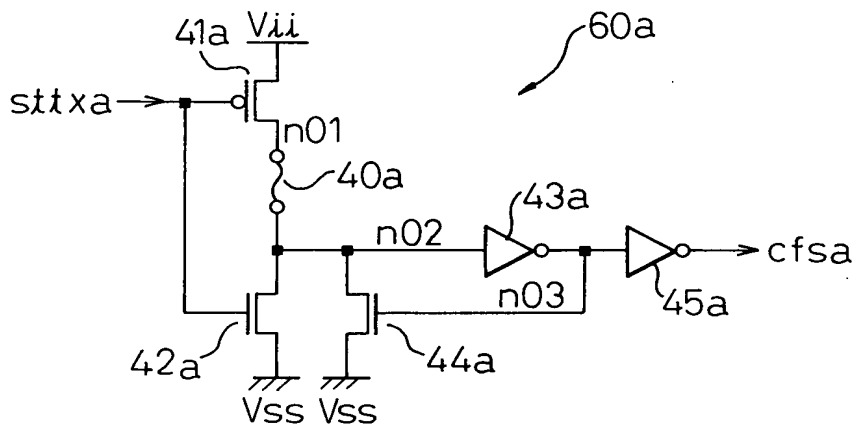
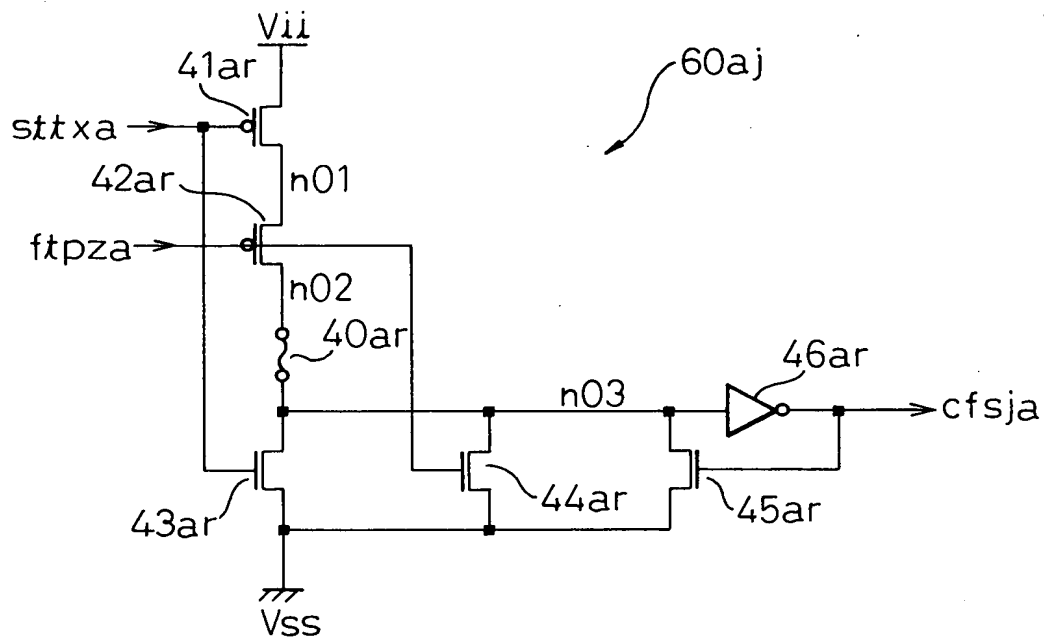


Fig.108



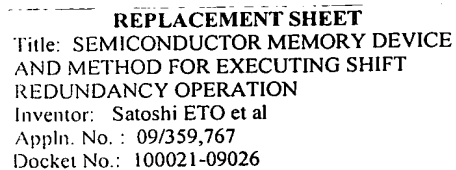

$$\frac{84}{87}$$

Fig.109

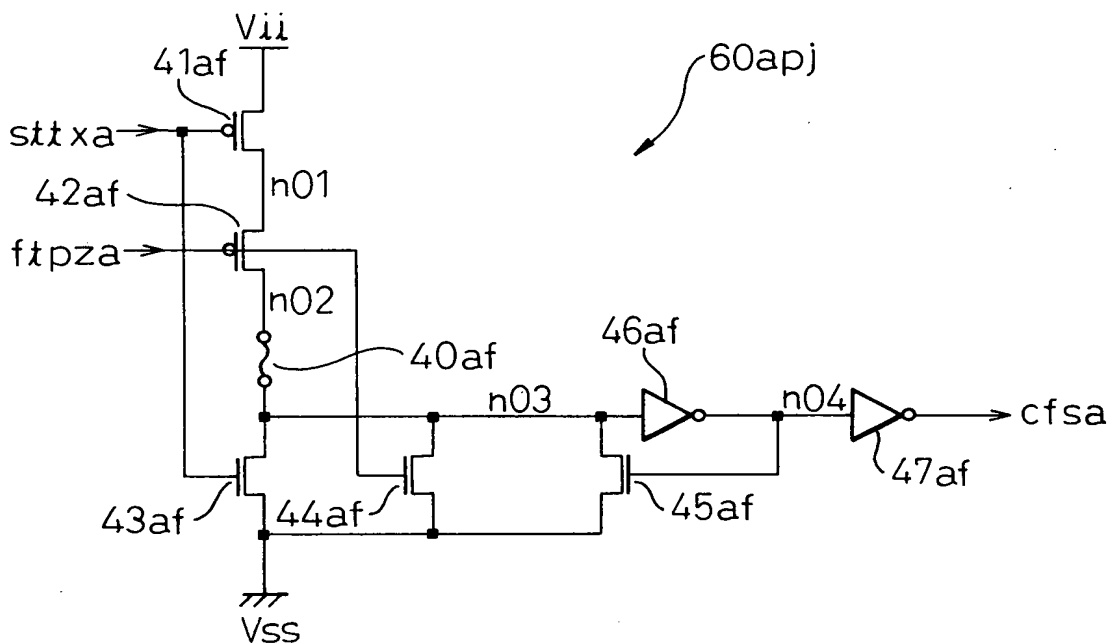
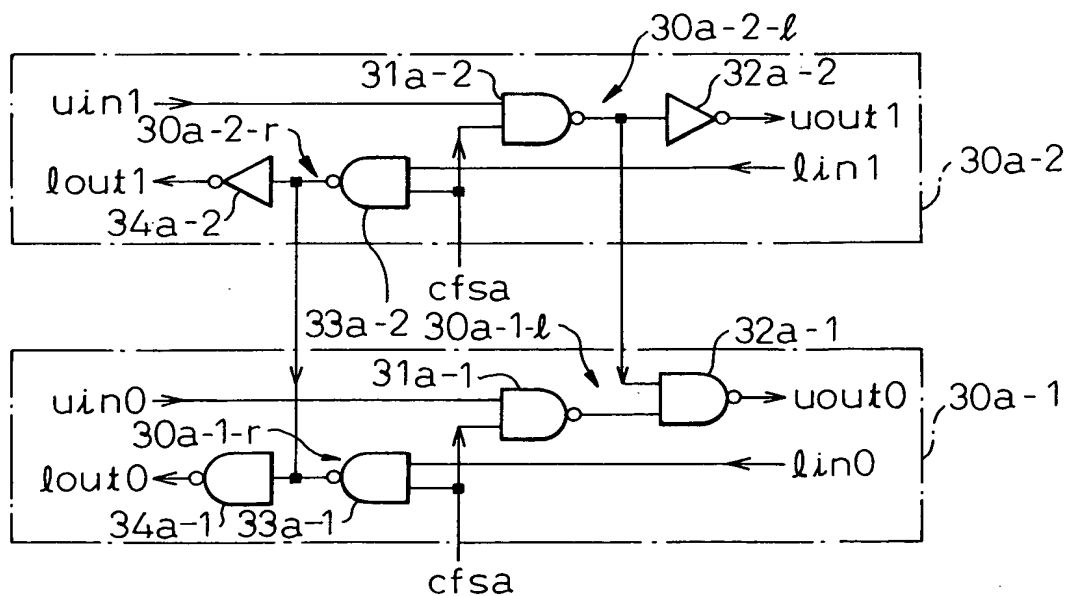


Fig.110





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Fig.111

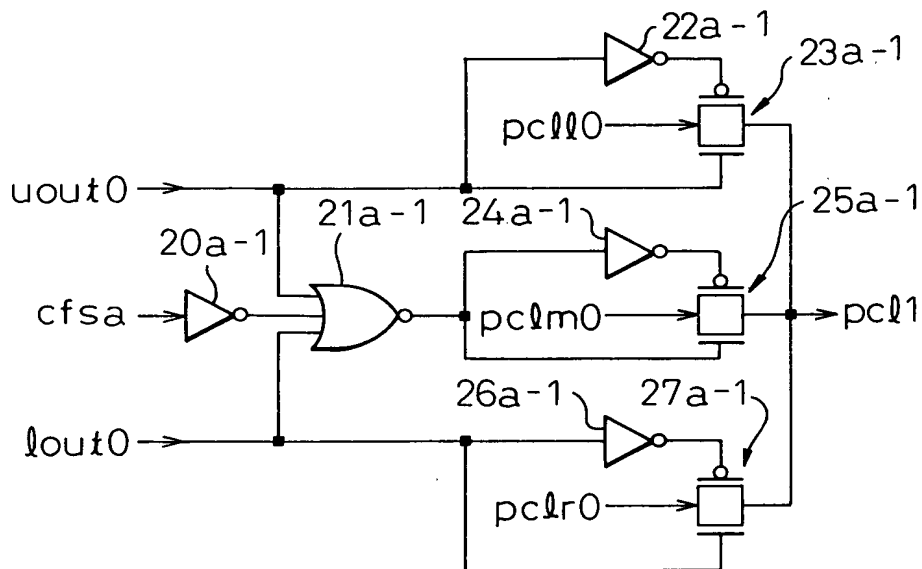
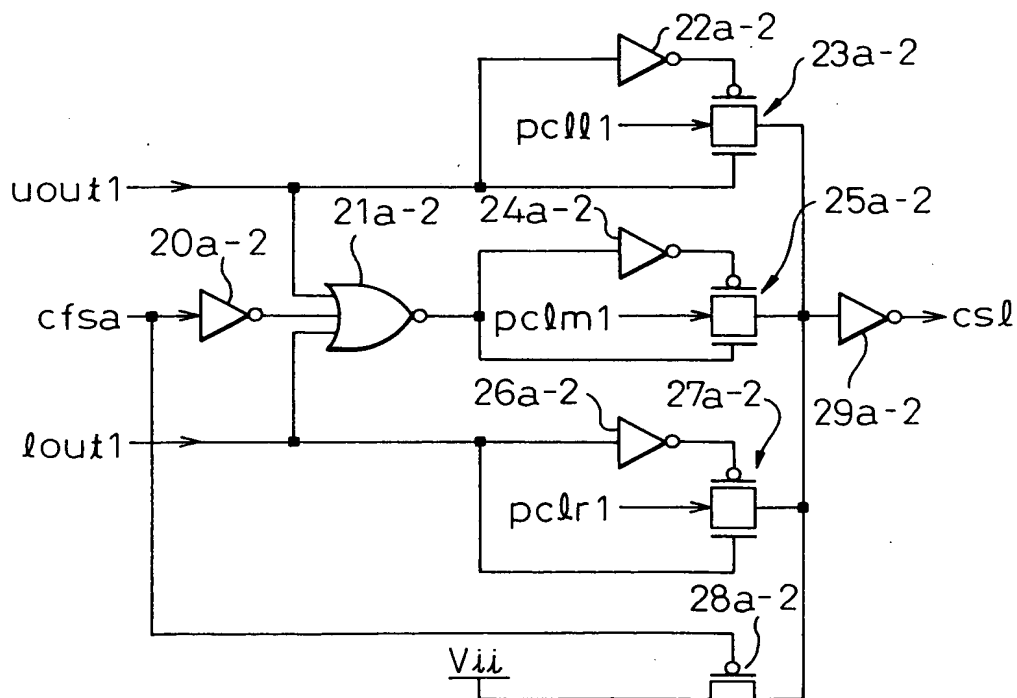


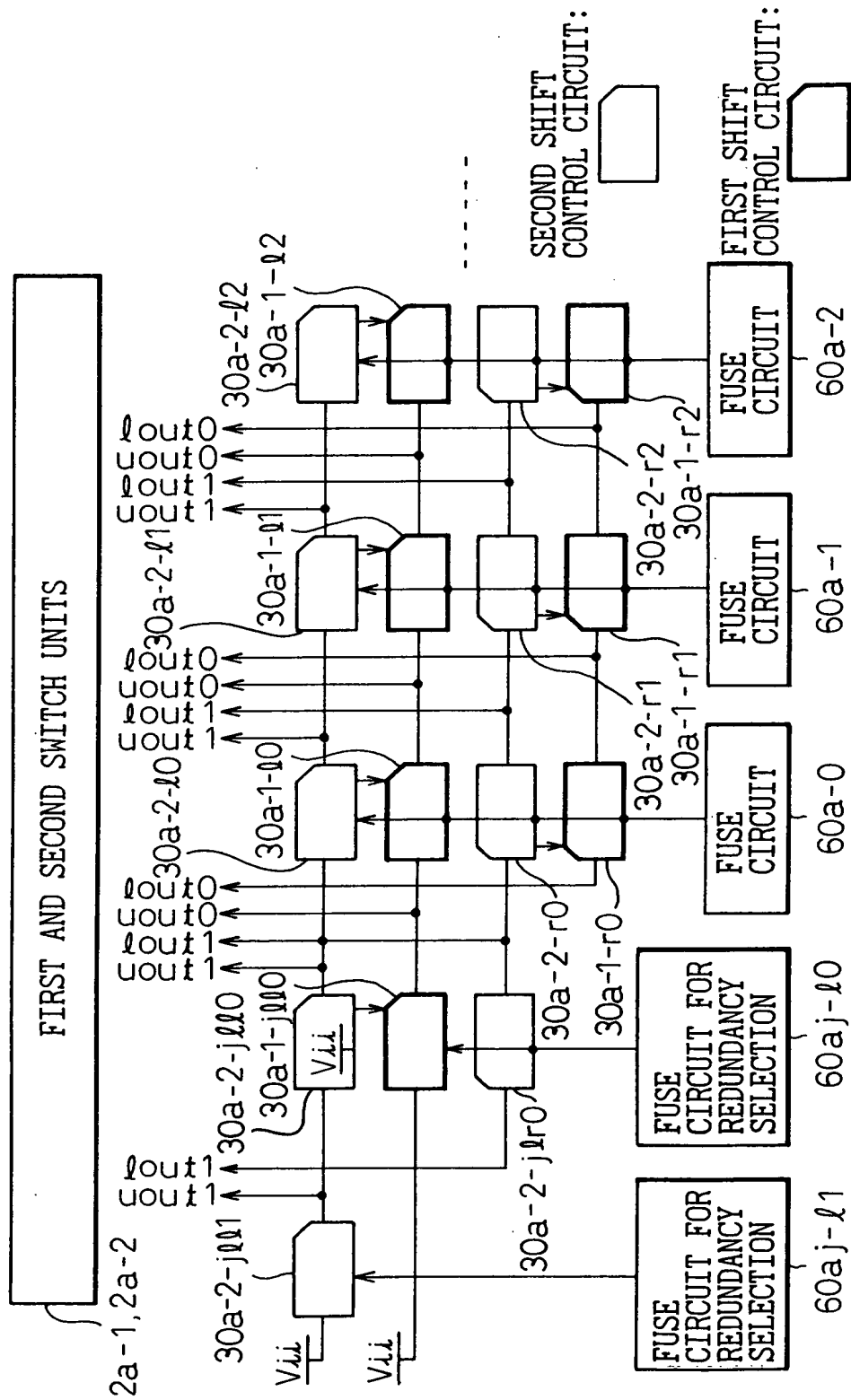
Fig.112





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Fig. 113



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Fig. 114

